OPTOMMP PROTOCOL GUIDE

Used with:
groov EPIC Processors
groov RIO modules
SNAP PAC R-Series Controllers
SNAP PAC S-Series Controllers
SNAP PAC EB Brains
SNAP PAC SB Brains
SNAP Simple I/O™
SNAP Ethernet I/O™
SNAP Ultimate I/O™
SNAP-LCE Controller
E1 Brain Board
E2 Brain Board
G4EB2 Brain Boards

Form 1465-200714—July 2020

OPTO 22
The Future of Automation.

OptoMMP Protocol Guide
Form 1465-200714—July 2020

The information in this manual has been checked carefully and is believed to be accurate; however, Opto 22 assumes no responsibility for possible inaccuracies or omissions. Specifications are subject to change without notice.

Opto 22 warrants all of its products to be free from defects in material or workmanship for 30 months from the manufacturing date code. This warranty is limited to the original cost of the unit only and does not cover installation, labor, or any other contingent costs. Opto 22 I/O modules and solid-state relays with date codes of 1/96 or newer are guaranteed for life. This lifetime warranty excludes reed relay modules, *groov* and SNAP serial communication modules, SNAP PID modules, and modules that contain mechanical contacts or switches. Opto 22 does not warrant any product, components, or parts not manufactured by Opto 22; for these items, the warranty from the original manufacturer applies. Refer to Opto 22 form 1042 for complete warranty information.

Opto 22
Automation Made Simple.

Table of Contents

1: Introduction

WELCOME TO OPTOMMP

OptoMMP is a memory-mapped protocol based on the IEEE 1394 standard. This protocol is used to create custom software applications for remote monitoring, industrial control, and data acquisition using Opto 22 hardware products.

If your sole method of communication with Opto 22 devices is through a PAC Control Basic or PAC Control Professional strategy, then you probably don't need to use this programming guide. Instead, the *PAC Control User's Guide* (form 1700) or the *PAC Control User's Guide, Legacy Edition* (form 1710) for legacy hardware will provide the information you need.

However, if you are developing custom applications for your Opto 22 devices, either instead of or in addition to using PAC Control or other methods of communication, you'll need the additional information provided in this protocol guide.

OptoMMP works with the following Opto 22 hardware products:

Device type	Part numbers	
groov EPIC processors	GRV-EPIC-PR1	
groov RIO modules	GRV-R7-MM1001-10	
SNAP PAC R-series on-the-rack controllers	SNAP-PAC-R1 SNAP-PAC-R1-B SNAP-PAC-R1-FM SNAP-PAC-R1-W	SNAP-PAC-R2 SNAP-PAC-R2-FM SNAP-PAC-R2-W
SNAP PAC S-series standalone controllers	SNAP-PAC-S1 SNAP-PAC-S1-FM SNAP-PAC-S1-W	SNAP-PAC-S2 SNAP-PAC-S2-W
SNAP PAC EB brains	SNAP-PAC-EB1 SNAP-PAC-EB1-FM SNAP-PAC-EB1-W	SNAP-PAC-EB2 SNAP-PAC-EB2-FM SNAP-PAC-EB2-W
SNAP PAC SB brains	SNAP-PAC-SB1	SNAP-PAC-SB2
SNAP Simple I/O	SNAP-ENET-S64	
SNAP Ethernet I/O	SNAP-B3000-ENET SNAP-ENET-RTC	SNAP-ENET-D64
SNAP Ultimate I/O	SNAP-UP1-ADS SNAP-UP1-M64	SNAP-UP1-D64
SNAP-LCE standalone controller	SNAP-LCE	
E1 digital brain board	E1	
E2 analog brain board	E2	

Device type	Part numbers	
G4EB2 brain boards	G4EB2 G4D32EB2	G4D32EB2-UPG

ABOUT THIS GUIDE

This user's guide defines the OptoMMP protocol and includes the logical addresses for communicating with Opto 22's OptoMMP-based hardware.

It assumes that you are already familiar with programming in the format you've chosen to use. If you are using our free OptoMMP SDKs, you'll find documentation included in the download.

The guide also assumes that you have already installed the Opto 22 hardware. If you have not, see the hardware user's guide for instructions.

This guide includes the following sections:

Chapter 1: Introduction—information about the guide and how to reach Opto 22 Product Support.

Chapter 2: Overview of Programming—basic information you need for programming applications using the OptoMMP protocol.

Chapter 3: Using OptoMMP Software Development Kits—programming your own applications using our software development kits to hide the details of the memory map and the protocol.

Chapter 4: Using the OptoMMP Protocol—details of the OptoMMP protocol, including examples.

Appendix A: Opto 22 Hardware Memory Map—the complete memory map for Opto 22 devices using the OptoMMP protocol.

Appendix B: Rack and Module Compatibility—a table listing part numbers, mounting racks, and the type and number of I/O modules they can hold by product family.

Information Key

This guide includes information that applies to some types of Opto 22 memory-mapped products but not to others. Sections are marked as follows to indicate the products that support them:

This text	Indicates support by this hardware
PR1	*groov* EPIC PR1 processor
RIO	groov RIO modules
PAC-R	SNAP PAC R-series controllers
PAC-S	SNAP PAC S-series controllers
EB	SNAP PAC EB brains
SB	SNAP PAC SB brains
UIO	SNAP Ultimate I/O
EIO	SNAP Ethernet I/O
SIO	SNAP Simple I/O
LCE	SNAP-LCE controllers*
E1	E1 brain boards
E2	E2 brain boards
G4EB2	G4EB2 brain boards

*As of January 2014, the SNAP-LCE is no longer available due to unavailability of essential parts.

Other Documents You May Need

See the following additional guides for the information listed. Most guides are available on our website, www.opto22.com; those that are not on the website are available with product purchase. The easiest way to find a guide is to search on its form number.

For this information	See this guide	Form #
Installing and using *groov* EPIC processors, *groov* modules, and *groov* Manage software	*groov EPIC User's Guide*	2267
Installing and using groov RIO modules	*groov RIO User's Guide*	2324
Installing and using a SNAP PAC R-series controller	*SNAP PAC R-Series Controller User's Guide*	1595
Installing and using a SNAP PAC S-series controller	*SNAP PAC S-Series Controller User's Guide*	1592
Installing and using a SNAP PAC EB or SB brain	*SNAP PAC Brains User's Guide*	1690
Installing and using a SNAP Ultimate, SNAP Ethernet, or SNAP Simple I/O unit	*SNAP Ethernet-Based I/O Units User's Guide*	1460
Installing and using a SNAP-LCE controller	*SNAP-LCE User's Guide*	1475
Installing and using an E1 or E2 brain board	*EI and E2 User's Guide*	1563
(For SNAP PAC Systems only) Assigning IP addresses to SNAP PAC hardware, configuring communications, doing real-time reads and writes, updating firmware. For PAC-R, EB, SB, UIO, EIO, SIO, E1/E2, and G4EB2 units, configuring I/O channels[a] and system functions.	*PAC Manager User's Guide, Legacy Edition*	1714
Designing flowchart-based control programs for the system (Requires a *groov* EPIC processor or SNAP PAC controller; SNAP-LCE and SNAP Ultimate controllers are partially supported)	*PAC Control User's Guide*	1700
	PAC Control Command Reference	1701
	PAC Control Commands Quick Reference	1703
Communicating with the system using OPC	*OptoOPCServer User's Guide* (included with the purchase of OptoOPCServer)	1439
Exchanging system data with popular databases	*OptoDataLink User's Guide* (included with the purchase of OptoDataLink)	1705
Communicating with Allen-Bradley Logix-based PLCs or other systems using EtherNet/IP	*EtherNet/IP for SNAP PAC Protocol Guide*	1770
Communicating with systems using Modbus/TCP	*Modbus/TCP Protocol Guide*	1678
Communicating with an E1 or E2 I/O unit using the Optomux protocol	*Optomux Protocol Guide*	1572

[a] This guide uses the terms *point* and *channel* interchangeably.

FOR HELP

If you have problems using the OptoMMP protocol and cannot find the help you need in this guide or on our website, contact Opto 22 Product Support.

Phone: 800-TEK-OPTO (800-835-6786 toll-free in the U.S. and Canada)
951-695-3080
Monday through Friday,
7 a.m. to 5 p.m. Pacific Time

NOTE: Email messages and phone calls to Opto 22 Product Support are grouped together and answered in the order received.

Fax: 951-695-3017

Email: support@opto22.com

Opto 22 website: www.opto22.com

When calling for technical support, you can help us help you *faster* if you provide the following information to the Product Support engineer:

- A screen capture of the Help > About dialog box showing software product and version (available by clicking Help > About in the application's menu bar).
- Opto 22 hardware part numbers or models that you're working with.
- Firmware version (Available in PAC Manager by clicking Tools > Inspect. Available in *groov* Manage by clicking Info and Help > About.)
- Specific error messages you saw.
- Version of your computer's operating system.

2: Overview of Programming

INTRODUCTION

Details of programming steps depend on the language or method you use for developing your custom application, but some basic information is common to all languages and methods. This chapter includes the following basic information you need in order to program for Opto 22 memory-mapped hardware:

In this chapter

PROGRAMMING STEPS FOR OPTO 22 DEVICES

In general, writing programs that can read from or write to Opto 22 memory-mapped devices through OptoMMP memory maps involves six steps:

1. Connect to the device (not required for UDP).
2. Send a powerup clear (PUC) to the device.
3. Configure channels[1] and channel features. (For instructions, see page 16).
4. (Optional) Configure event/reactions, security, streaming, and other functions (starting on page 39).

   NOTE: Store configurations to flash memory if you want them to remain through power cycles.

5. Read and write to channels.
6. Disconnect from the device (not required for UDP). This step occurs only after all communication is finished. The connection is left open during normal communications.

Before you start using OptoMMP, here is some important information you should understand about Opto 22 memory-mapped devices, I/O modules, and I/O channels.

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[1] This guide uses the terms *point* and *channel* interchangeably.

COMMUNICATION OPTIONS

PR1
RIO
PAC-R
PAC-S
EB
SB
UIO
EIO
SIO
LCE
E1
E2
G4EB2

To communicate with Opto 22 devices, you can use the OptoMMP protocol either by itself or in combination with other communication methods. For example, your system could be running a PAC Control strategy, providing data to a peer on the network, and communicating with a third-party HMI, all at the same time.

Communication options include:

Custom applications for Microsoft Windows® and Linux®—You can use the OptoMMP protocol to build custom applications from scratch. For details, see Chapter 4: Using the OptoMMP Protocol.

However, you can quick start your development process with two free Opto 22 software development kits (SDKs), which you can download from our website at www.opto22.com:

- For C++®—the PAC-DEV-OPTOMMP-CPLUS software development kit (SDK).
  The SDK supports Microsoft Windows® and Linux, and includes all documentation.
- For Visual Studio® 2010 through 2019—the PAC-DEV-OPTOMMP-DOTNET SDK for .NET developers. The SDK supports Microsoft's .NET frameworks 4.0 through 4.8, and includes all documentation.

  A *groov* Enterprise license is required to run custom applications on a *groov* EPIC processor. For details, see the *groov EPIC User's Guide*, (form 2267), available from the Opto 22 website.

Communication Options that Do Not Require the OptoMMP Protocol

None of the following communication options requires knowledge of the OptoMMP protocol:

PAC Control™—Most of the devices that use the OptoMMP protocol can be used with PAC Control, Opto 22's flowchart-based control development software. PAC Control Basic is included in your purchase of a *groov* EPIC processor or SNAP PAC controller, and is also a free download from www.opto22.com. PAC Control Professional adds more features and is available for purchase from our website or through an Opto 22 distributor.

CODESYS® Development System—(*groov* EPIC Systems only) *groov* EPIC processors can be programmed using any IEC 61131-3 compliant language in CODESYS. For more information, see the *groov EPIC User's Guide*.

Ignition Edge®—(*groov* EPIC Systems only) *groov* EPIC processors include Ignition Edge® software from Inductive Automation® to connect to other devices, such as Allen-Bradley® PLCs, via OPC UA, and for efficient IIoT communications using MQTT with Sparkplug B payload.

Node-RED—(*groov* EPIC and *groov* RIO only) Node-RED, an open-source tool for communicating data among devices, databases, cloud applications, and APIs, is included in *groov* EPIC and *groov* RIO.

EtherNet/IP™—SNAP PAC controllers and SNAP PAC EB brains with firmware R8.3 and higher can also communicate with Allen-Bradley® Logix-based PLCs and other systems that use EtherNet/IP. For details, see the *EtherNet/IP for SNAP PAC Protocol Guide* (form 1770), available from our website.

Modbus®/TCP—Ethernet-based devices that use the OptoMMP protocol can also communicate using Modbus/TCP. For more information about communicating with Opto 22 devices using Modbus/TCP, see the *Modbus/TCP Protocol Guide* (form 1678), available from our website.

Optomux protocol—E1 and E2 brain boards can also communicate using the Optomux protocol over Ethernet or serial networks. The Optomux Protocol Driver is documented in the *Optomux Protocol Guide* (form 1572); the driver and the guide are available from our website.

Accessing Opto 22 Ethernet-Based Devices over the internet

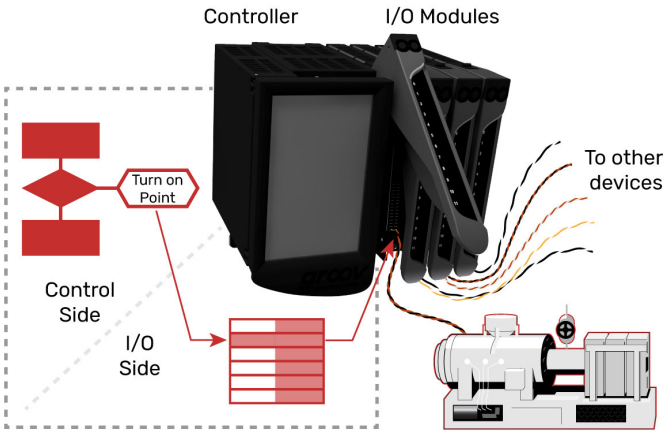
Since Opto 22 Ethernet-based devices are just like any other hardware on the Ethernet network, you can access them over the internet in exactly the same way you would access a computer; the details depend on

your network and internet connection. Consult your system or network administrator or your Internet Service Provider (ISP) for more information.

CAUTION: Multiple Communication Options Can Cause Conflict

Any time you directly communicate with an Opto 22 memory-mapped device, make sure that you are not causing conflicts with other communication options. For example, if you are using the memory map to exchange data with an I/O unit, and that I/O unit is also controlled by a PAC Control strategy, be careful that the two methods of reading and writing to the unit do not send conflicting directions to I/O. This caution applies to all Opto 22 devices that have multiple communication options.

Some Opto 22 memory-mapped devices—*groov* EPIC processors, SNAP PAC R-series controllers, and SNAP Ultimate brains—are a combination of I/O processor and controller: they handle both input/output processing and flowchart-based control functions in the same device. Because input/output processing and control are different functions, it's sometimes easier to imagine these devices performing these tasks in different "sides": a control side and an I/O side.



This image depicts a GRV-EPIC-PR1 and *groov* I/O modules on a *groov* EPIC chassis. Together, these devices are referred to as an *I/O unit*.

The modules on the chassis connect with devices (such as the motor) to monitor and control them.

Monitoring and control are performed by sending messages (commands) to addresses in the *groov* EPIC processor's *memory map*.

On the control side, these Opto 22 devices have capabilities very much like a SNAP PAC S-series or SNAP-LCE standalone controller: they typically run a control program developed in PAC Control software. (Some, like *groov* EPIC, can run programs developed with other tools.) The control program provides the logic that controls processes throughout the system. Within the program, PAC Control commands (programming functions) read and write to the memory map in the I/O side to monitor and control I/O channels.

On the I/O side, these Opto 22 devices have features similar to a SNAP PAC EB brain or a SNAP Ethernet brain: they read and write to I/O channels by using the *memory map* (see "Understanding the Memory Map" on page 8).

***IMPORTANT**: Any time you are communicating with both the control side and the I/O side, plan carefully and use caution. The control side reads from and writes to the I/O side just as other methods do directly. Make sure that data being written directly to the I/O side does not conflict with control logic being executed in the main control program.*

UNDERSTANDING THE MEMORY MAP

NOTE: Appendix A: Opto 22 Hardware Memory Map shows all memory map addresses and the devices each section supports.

PR1
RIO
PAC-R
PAC-S
EB
SB
UIO
EIO
SIO
LCE
E1
E2
G4EB2

Opto 22 memory-mapped devices use the IEEE 1394 specification as a standard for reading and writing data. This standard specifies a memory-mapped model for devices on a network. Basically, each node (such as a SNAP PAC brain) appears logically as a 48-bit address space[2]. To communicate with a device, you read from and write to specific memory addresses in that space.

If you're a programmer, you already know that a memory map is a data structure that matches a set of logical addresses with physical addresses in the read/write memory hardware on a device. You can think of a memory map as a lookup table, or if you're familiar with programmable logic controllers (PLCs), it's similar to a PLC's register.

In Opto 22 memory-mapped devices, a physical address might hold a single value of data, such as the state of a single digital channel, counter data for a digital channel, the minimum value of an analog channel, or the device's firmware version. In your programming code, you use the logical address to reference the physical address that holds the data you want to read or write to.

When you write to the memory map, the memory-mapped device responds by returning a packet that indicates success or a failure code. When you perform a read, the memory-mapped device returns a packet containing the data.

If you're not a programmer, you can think of a memory map (sometimes called a *mem map*) as a collection of post office boxes. Each mailbox's address has a different owner who either has information you want, or information you want to change.

To get or change the information, you send a message (in the form of a structured packet of data) to the mailbox address. For example, to get a device's part number, you send the message to address **FFFF F030 0080**. In response, you'll get another packet of data containing—in this example—the part number. Getting a part number is an example of *reading* a memory map address. You can also *write* to the memory map, for example, to change an I/O channel's configuration, its status, or its value.

Note that devices vary in how much of the memory map they support. For example, the SNAP PAC S-series standalone controller does not support reading or writing to channels, since it is not directly connected to channels. Similarly, a digital-only brain does not support analog sections of the memory map.

Also note that features included in the memory map may not always be the same as features available through another protocol. For example, waveform generation is supported on an E2 using the Optomux protocol, but it is not available on an E2 in OptoMMP. For a list of features supported by each device, see Appendix C: SNAP Features Comparison Chart and Appendix D: groov EPIC and groov RIO Features and Comparison Charts.

[2] 48 bits is equivalent to 6 octets. `FFFF F110 0000` is an example of a 48-bit address space.

REFERENCING MODULE AND CHANNEL POSITIONS ON I/O UNITS

PR1
RIO
PAC-R
PAC-S
EB
SB
UIO
EIO
SIO
LCE
E1
E2
G4EB2

NOTE: You can use the reference model described in this section by all methods of communication listed in "Communication Options" on page 6 except *Modbus/TCP and Optomux. For Modbus I/O channel referencing, see the Modbus chapter in the* Modbus/TCP Protocol Guide *(form 1678). For Optomux, see the* Optomux Protocol Guide *(form 1572).*

Before you begin writing programs that read and write to the memory map addresses in Appendix A: Opto 22 Hardware Memory Map, you first need to know how to reference I/O modules and the channels on them.

Opto 22 I/O units are zero-based: that is, the first module position on the rack or chassis is position 0, and the first channel on each module is channel 0. The number of channels on a module can vary from one to 32, depending on the module family and part number. Because of this numbering and variation, it's important to understand them before you start reading and writing channel data.

Module and channel positions differ depending on the module family; see the section for yours:

For serial modules, also see page 107.

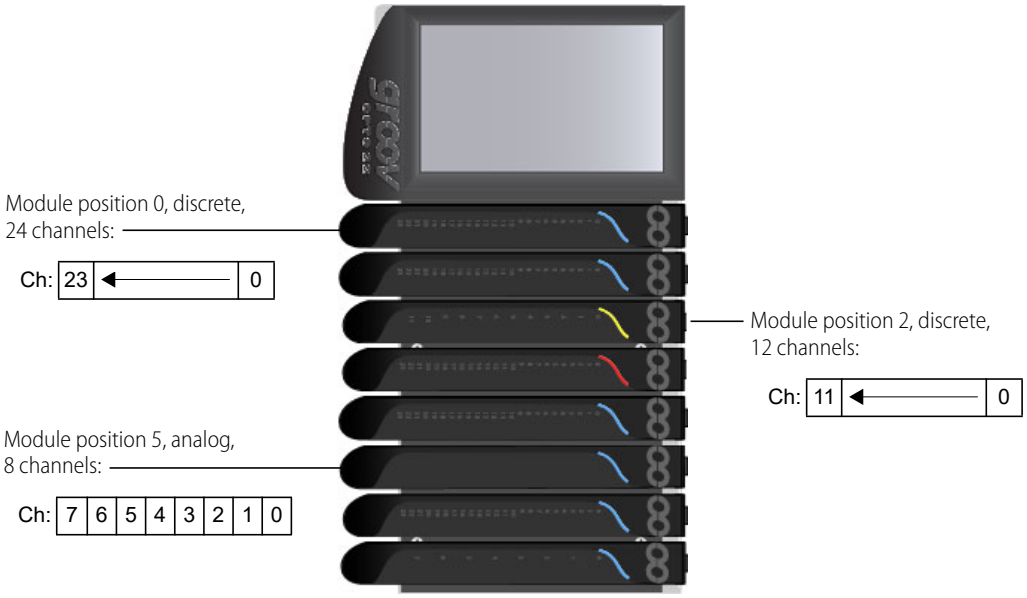
PR1

groov I/O Units

I/O units whose I/O processor is a GRV-EPIC-PR1 are called *groov* I/O units. *groov* I/O chassis can hold 4, 8, or 16 I/O modules, and each module contains 8 to 24 channels, depending on the module. Several *groov* modules offer a variety of features that you can configure. After you learn how to reference module and channel positions, then continue to configuring channels and features:

- To configure *groov* I/O channels, see page 16
- To configure *groov* I/O features, see page 31.

The following diagram shows examples of *groov* modules mounted on a chassis, along with the processor. The diagram also shows examples of how channels are identified on some of the modules.



RIO

groov RIO Units

A *groov* RIO module contains an I/O and communications processor plus a specific number of multifunction, multi-signal I/O channels. Multifunction means channels can be configured as either inputs or outputs; multi-signal means channels can be configured for different signal inputs. For example, the *groov* RIO part number GRV-R7-MM1001-10 includes a processor and ten I/O channels, eight of which are software configurable as analog or discrete inputs or outputs with a variety of signals, and two of which are Form C mechanical relays.

All channels on a *groov* RIO module are considered to be in module position 0. Channel positions are:

GRV-R7-MM1001-10
Channel Positions

Module position = 0

Pins	Channel
1–3	0
4–6	1
7–9	2
10–12	3
13–14	4
15–16	5
17–18	6
19–20	7
21–-23	8
24–26	9

To configure channels, see page 20.

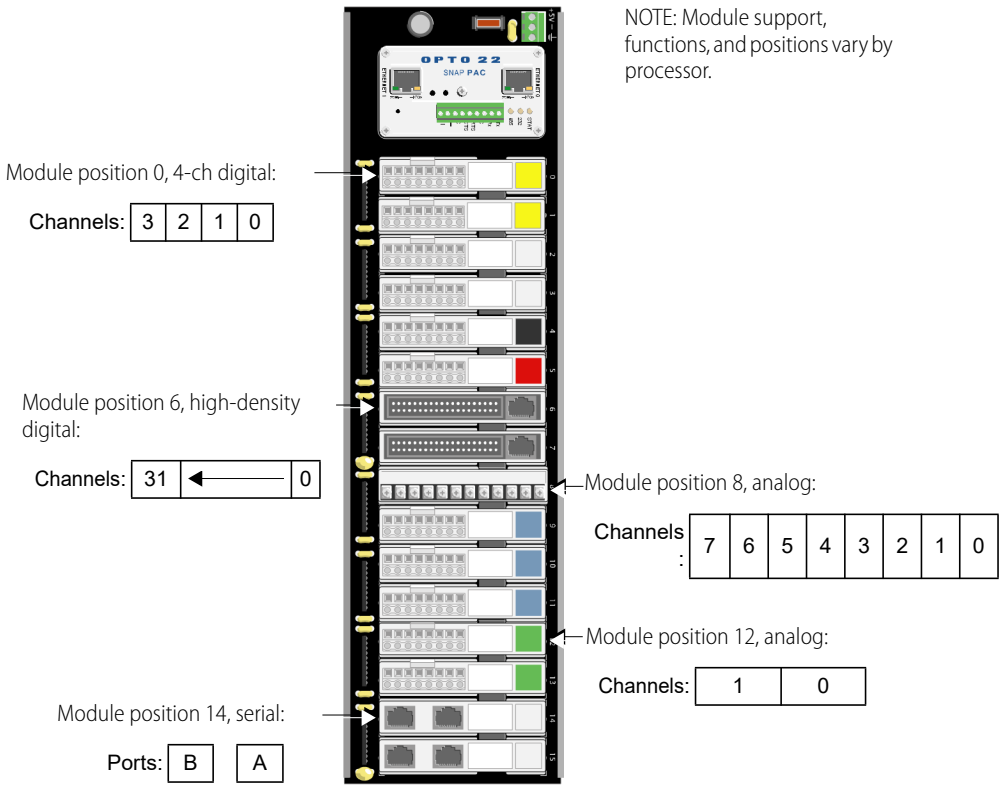
To configure channel features, see page 31.

PAC-R
EB
SB
UIO
EIO
SIO

SNAP I/O Units

I/O units whose I/O processor's part number begins with "SNAP" are called SNAP I/O units. For example, I/O units with a SNAP-PAC-R1, SNAP-EB1, or SNAP-ENET-S64 as the I/O processor are all SNAP I/O units.

SNAP mounting racks may hold 4, 8, 12, or 16 I/O modules, and the modules can be analog, digital, or serial. Each module contains 1 to 32 channels (points), depending on the module. Examples of modules are shown in the following diagram.

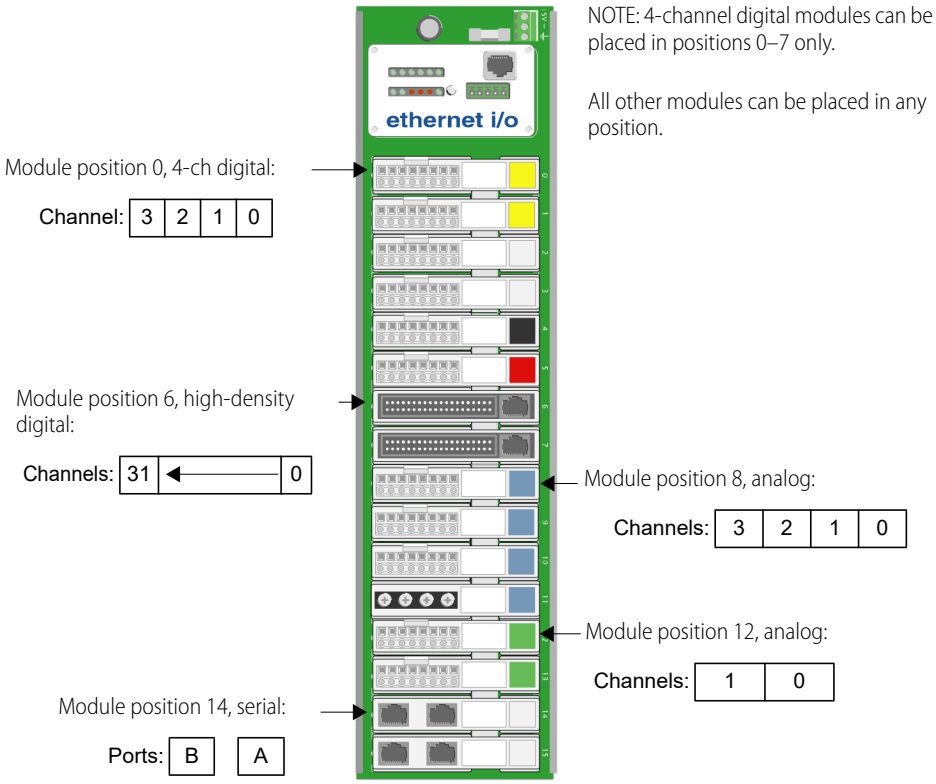


For more information about SNAP I/O channels, see page 21; for SNAP I/O features, see page 31.

SNAP B-Series I/O Units

NOTE: SNAP B-series racks and the processors compatible with them are not recommended for new development. Use SNAP PAC racks and processors instead.

SNAP B-series mounting racks can hold up to 4, 8, 12, or 16 Opto 22 SNAP I/O modules. (Not all modules are supported by these processors; for details, see *Legacy and Current SNAP Product Comparison and Compatibility Charts,* form 1693.) Analog, serial, and high-density digital modules (digital modules with more than four channels) can be placed in any position. For the larger racks, 4-channel digital modules can be placed in positions 0–7 only. Each module contains 1 to 32 channels, depending on the module. Examples of modules are shown in the following diagram.



SNAP Digital-Only I/O Units

NOTE: Digital-only racks and processors are not recommended for new development. Use SNAP PAC racks and processors instead.

The SNAP-D64RS mounting rack is compatible with SNAP-UP1-D64 and SNAP-ENET-D64 processors. The rack holds up to 16 4-channel SNAP digital I/O modules. Analog, serial, and high-density digital modules are not supported. Module position 0 is the position closest to the processor.

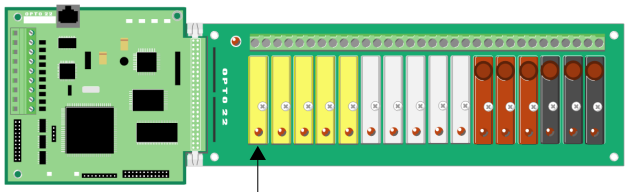
E1
E2

E1 and E2 I/O Units

I/O units using a digital E1 or analog E2 brain board normally use modules containing only one channel, and the maximum number of channels on the rack is 16. Examples of E1 and E2 I/O units are shown below.

E1 shown with G4 modules.

Since each module has just one channel, use only the first channel for each module in the memory map.



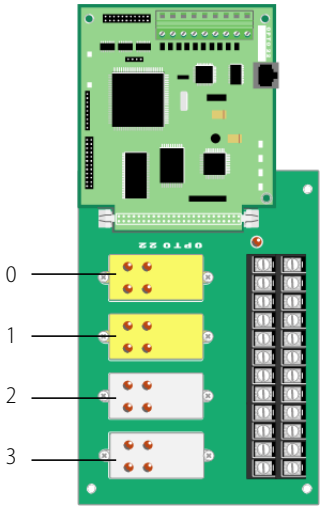
Module position 0

Module #	Channel #
00 ↓ 15	0 ↓ 0

E1 with Quad Pak modules.

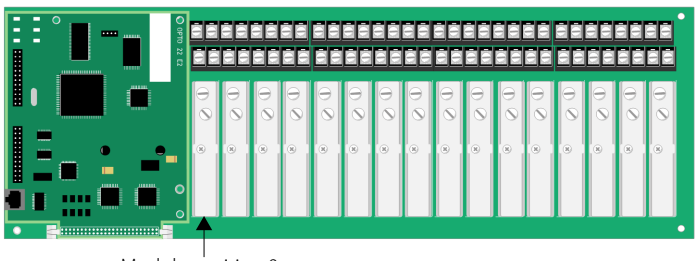
Quad Pak modules have four input or four output channels, but each channel is treated as if it were a separate one-channel module.

Module position on Quad Pak rack	Module number	Channel number
0	00 01 02 03	0 0 0 0
1	04 05 06 07	0 0 0 0
2	08 09 10 11	0 0 0 0
3	12 13 14 15	0 0 0 0



E2 with G1 modules.

Since each module has just one channel, use only the first channel for each module in the memory map.



Module position 0

Module #	Channel #
00 ↓ 15	0 ↓ 0

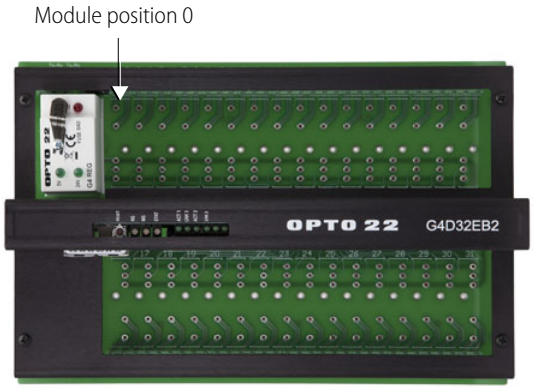
G4EB2

G4EB2 I/O Units

These I/O units include part numbers G4EB2, G4D32EB2, and G4D32EB2-UPG. Each I/O unit has 32 total channels, all of them digital. They may use G4 modules, which each have one channel, or Quad Pak modules, which each have four channels of the same type (all four digital inputs or all four digital outputs).

G4EB2 brains with G4 modules

Each module has just one channel (point). However, in the memory map they are addressed like Quad Pak racks (see page 15). The difference is that with G4s, you can mix input and output modules within the same group of four channels.



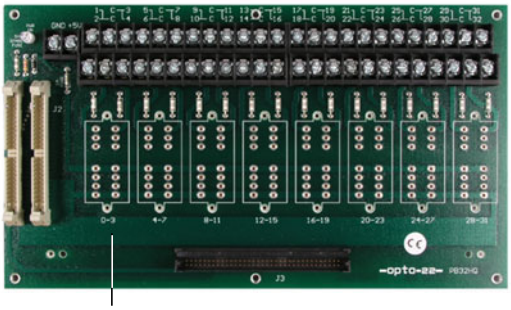
The following table shows Channel Configuration addresses as an example of how to reference channels on a rack with G4 modules.

G4 rack	Memory Map equivalent		
Module position	Module number	Channel number	Starting address for channel config
0	0	0	F010 0000
1	0	1	F010 00C0
2	0	2	F010 0180
3	0	3	F010 0240
4	1	0	F010 3000
5	1	1	F010 30C0
6	1	2	F010 3180
7	1	3	F010 3240
8	2	0	F010 6000
9	2	1	F010 60C0
10	2	2	F010 6180
11	2	3	F010 6240
12	3	0	F010 9000
13	3	1	F010 90C0
14	3	2	F010 9180
15	3	3	F010 9240
16	4	0	F010 C000
17	4	1	F010 C0C0
18	4	2	F010 C180
19	4	3	F010 C240
20	5	0	F010 F000
21	5	1	F010 F0C0
22	5	2	F010 F180
23	5	3	F010 F240

G4 rack	Memory Map equivalent		
Module position	Module number	Channel number	Starting address for channel config
24	6	0	F011 2000
25	6	1	F011 20C0
26	6	2	F011 2180
27	6	3	F011 2240
28	7	0	F011 5000
29	7	1	F011 50C0
30	7	2	F011 5180
31	7	3	F011 5240

G4EB2 brains with Quad Pak modules

Quad Pak modules have four input or four output channels per module, so each group of four channels must be configured as either inputs or outputs.



Module position 0 (channels 0–3)

The following table shows Channel Configuration addresses as an example of how to reference channels on a PB32HQ rack with Quad Pak modules.

Quad Pak rack		Memory Map equivalent		
Module position	Channel number	Module number	Channel number	Starting address for channel config
0	0	0	0	F010 0000
	1	0	1	F010 00C0
	2	0	2	F010 0180
	3	0	3	F010 0240
1	4	1	0	F010 3000
	5	1	1	F010 30C0
	6	1	2	F010 3180
	7	1	3	F010 3240
2	8	2	0	F010 6000
	9	2	1	F010 60C0
	10	2	2	F010 6180
	11	2	3	F010 6240
3	12	3	0	F010 9000
	13	3	1	F010 90C0
	14	3	2	F010 9180
	15	3	3	F010 9240
4	16	4	0	F010 C000
	17	4	1	F010 C0C0
	18	4	2	F010 C180
	19	4	3	F010 C240

Quad Pak rack		Memory Map equivalent		
Module position	Channel number	Module number	Channel number	Starting address for channel config
5	20	5	0	F010 F000
	21	5	1	F010 F0C0
	22	5	2	F010 F180
	23	5	3	F010 F240
6	24	6	0	F011 2000
	25	6	1	F011 20C0
	26	6	2	F011 2180
	27	6	3	F011 2240
7	28	7	0	F011 5000
	29	7	1	F011 50C0
	30	7	2	F011 5180
	31	7	3	F011 5240

CONFIGURING I/O CHANNELS

Before you can read or write to I/O channels, you must make sure channel types and channel features are configured as required.

See the section for your I/O unit:

PR1

Configuring I/O Channels for *groov* I/O Units

You can configure *groov* I/O units in three ways:

- PAC Control—If you are programming a strategy with PAC Control (R10.0 or higher), configure channels while you are programming the strategy.
- ***groov*** Manage—If your control program is not a PAC Control strategy, configure channels in *groov* Manage, either on the *groov* EPIC processor's touchscreen or remotely from a computer or mobile device. Configurations are automatically saved to flash memory.
- OptoMMP—If OptoMMP is the ONLY communication to the *groov* I/O unit, then configure I/O channels by selecting the appropriate configuration values as described below.

groov I/O Module Types and Channel Types

The table beginning on page 17 shows configuration values for *groov* I/O modules, divided by module and channel types.

- Some modules provide or accept several ranges of values per channel, which is why they have multiple channel types. If a module offers more than one range, choose the range you want from the Description column and read across to the Channel ID (hex) column to find the corresponding configuration value. For example, suppose the module in position (slot) 0 on the chassis is a GRV-IV-24 and you want to monitor a range of ±10 V on the first two channels (channels 0 and 1). You find the module's range in the Description column and read across to see that the appropriate configuration value is 0x60000017.
- Some modules provide or accept only certain configuration values on specific channels. Those modules list the specific channel that accepts a specific configuration value in the "Applies To" column. If the

column says "all", that means all channels on that module accept all the configuration values available for that module.

After you select the configuration value for the module and channel type, go to page 31 to select the correct configuration value for a specific feature.

Part number	Applies To	Description	Module ID (hex)	Channel ID (hex)	Channels per module	Default Units	Low Scale	Full Scale
GRV-CSERI-4	all	RS232	0C00001E	08000026	4	N/A	N/A	N/A
GRV-CSERI-4	all	RS485, 2-Wire, no termination, no bias	0C00001E	08000027	4	N/A	N/A	N/A
GRV-CSERI-4	all	RS485, 2-Wire, termination, no bias	0C00001E	08000028	4	N/A	N/A	N/A
GRV-CSERI-4	all	RS485, 2-Wire, no termination, bias	0C00001E	08000029	4	N/A	N/A	N/A
GRV-CSERI-4	all	RS485, 2-Wire, termination, bias	0C00001E	0800002A	4	N/A	N/A	N/A
GRV-CSERI-4	all	RS485, 4-Wire, no termination, no bias	0C00001E	0800002B	4	N/A	N/A	N/A
GRV-CSERI-4	all	RS485, 4-Wire, termination, no bias	0C00001E	0800002C	4	N/A	N/A	N/A
GRV-CSERI-4	all	RS485, 4-Wire, no termination, bias	0C00001E	0800002D	4	N/A	N/A	N/A
GRV-CSERI-4	all	RS485, 4-Wire, termination, bias	0C00001E	0800002E	4	N/A	N/A	N/A
GRV-IAC-24	all	Digital Input	5000000F	50000000	24	N/A	N/A	N/A
GRV-IACDCTTL-24	all	Digital Input	50000005	50000000	24	N/A	N/A	N/A
GRV-IACDCTTLS-24	all	Simple Digital Input	54000007	54000000	24	N/A	N/A	N/A
GRV-IACHV-24	all	Digital Input	50000010	50000000	24	N/A	N/A	N/A
GRV-IACHVS-24	all	Simple Digital Input	54000008	54000000	24	N/A	N/A	N/A
GRV-IACI-12	all	Digital Input	5000000C	50000000	12	N/A	N/A	N/A
GRV-IACIHV-12	all	Digital Input	5000000D	50000000	12	N/A	N/A	N/A
GRV-IACIHVS-12	all	Simple Digital Input	54000009	54000000	12	N/A	N/A	N/A
GRV-IACIS-12	all	Simple Digital Input	5400000A	54000000	12	N/A	N/A	N/A
GRV-IACS-24	all	Simple Digital Input	5400001D	54000000	24	N/A	N/A	N/A
GRV-IDC-24	all	Digital Input	50000011	50000000	24	N/A	N/A	N/A
GRV-IDCI-12	all	Digital Input	5000000E	50000000	12	N/A	N/A	N/A
GRV-IDCIFQ-12	0	Digital Input with Quadrature	5000001A	5000002F	12	N/A	N/A	N/A
GRV-IDCIFQ-12	1	Digital Input with Quadrature	5000001A	5000002F	12	N/A	N/A	N/A
GRV-IDCIFQ-12	2	Digital Input with Quadrature Index	5000001A	50000030	12	N/A	N/A	N/A
GRV-IDCIFQ-12	3	Digital Input with Quadrature	5000001A	5000002F	12	N/A	N/A	N/A
GRV-IDCIFQ-12	4	Digital Input with Quadrature	5000001A	5000002F	12	N/A	N/A	N/A
GRV-IDCIFQ-12	5	Digital Input with Quadrature Index	5000001A	50000030	12	N/A	N/A	N/A
GRV-IDCIFQ-12	6	Digital Input with Quadrature	5000001A	5000002F	12	N/A	N/A	N/A
GRV-IDCIFQ-12	7	Digital Input with Quadrature	5000001A	5000002F	12	N/A	N/A	N/A
GRV-IDCIFQ-12	8	Digital Input with Quadrature Index	5000001A	50000030	12	N/A	N/A	N/A
GRV-IDCIFQ-12	9	Digital Input with Quadrature	5000001A	5000002F	12	N/A	N/A	N/A
GRV-IDCIFQ-12	10	Digital Input with Quadrature	5000001A	5000002F	12	N/A	N/A	N/A
GRV-IDCIFQ-12	11	Digital Input with Quadrature Index	5000001A	50000030	12	N/A	N/A	N/A
GRV-IDCIS-12	all	Simple Digital Input	5400000B	54000000	12	N/A	N/A	N/A

Part number	Applies To	Description	Module ID (hex)	Channel ID (hex)	Channels per module	Default Units	Low Scale	Full Scale
GRV-IDCS-24	all	Simple Digital Input	54000016	54000000	24	N/A	N/A	N/A
GRV-IICTD-12	all	ICTD Temperature Probe	6000001F	60000031	12	°C	-270	150
GRV-IMA-24	all	±20 mA	60000001	60000014	24	mA	-20	20
GRV-IMA-24	all	0-20 mA	60000001	60000015	24	mA	0	20
GRV-IMA-24	all	4-20 mA	60000001	60000016	24	mA	4	20
GRV-IMAI-8	all	0-20 mA	60000020	60000015	8	mA	0	20
GRV-IMAI-8	all	4-20 mA	60000020	60000016	8	mA	4	20
GRV-ITM-12	all	±1200 mV	60000026	60000002	12	mV	-1200	1200
GRV-ITM-12	all	±600 mV	60000026	60000003	12	mV	-600	600
GRV-ITM-12	all	±300 mV	60000026	60000004	12	mV	-300	300
GRV-ITM-12	all	±150 mV	60000026	60000005	12	mV	-150	150
GRV-ITM-12	all	±75 mV	60000026	60000006	12	mV	-75	75
GRV-ITM-12	all	±50 mV	60000026	60000007	12	mV	-50	50
GRV-ITM-12	all	±25 mV	60000026	60000008	12	mV	-25	25
GRV-ITM-12	all	Type B Thermocouple (°C)	60000026	60000009	12	°C	0	1820
GRV-ITM-12	all	Type E Thermocouple (°C)	60000026	6000000C	12	°C	-270	1000
GRV-ITM-12	all	Type J Thermocouple (°C)	60000026	6000000E	12	°C	-210	1200
GRV-ITM-12	all	Type K Thermocouple (°C)	60000026	6000000F	12	°C	-270	1372
GRV-ITM-12	all	Type N Thermocouple (°C)	60000026	60000010	12	°C	-270	1300
GRV-ITM-12	all	Type R Thermocouple (°C)	60000026	60000011	12	°C	-50	1768
GRV-ITM-12	all	Type S Thermocouple (°C)	60000026	60000012	12	°C	-50	1768
GRV-ITM-12	all	Type T Thermocouple (°C)	60000026	60000013	12	°C	-270	400
GRV-ITMI-8	all	±1200 mV	60000006	60000002	8	mV	-1200	1200
GRV-ITMI-8	all	±600 mV	60000006	60000003	8	mV	-600	600
GRV-ITMI-8	all	±300 mV	60000006	60000004	8	mV	-300	300
GRV-ITMI-8	all	±150 mV	60000006	60000005	8	mV	-150	150
GRV-ITMI-8	all	±75 mV	60000006	60000006	8	mV	-75	75
GRV-ITMI-8	all	±50 mV	60000006	60000007	8	mV	-50	50
GRV-ITMI-8	all	±25 mV	60000006	60000008	8	mV	-25	25
GRV-ITMI-8	all	Type B Thermocouple (°C)	60000006	60000009	8	°C	0	1820
GRV-ITMI-8	all	Type E Thermocouple (°C)	60000006	6000000C	8	°C	-270	1000
GRV-ITMI-8	all	Type J Thermocouple (°C)	60000006	6000000E	8	°C	-210	1200
GRV-ITMI-8	all	Type K Thermocouple (°C)	60000006	6000000F	8	°C	-270	1372
GRV-ITMI-8	all	Type N Thermocouple (°C)	60000006	60000010	8	°C	-270	1300
GRV-ITMI-8	all	Type R Thermocouple (°C)	60000006	60000011	8	°C	-50	1768
GRV-ITMI-8	all	Type S Thermocouple (°C)	60000006	60000012	8	°C	-50	1768
GRV-ITMI-8	all	Type T Thermocouple (°C)	60000006	60000013	8	°C	-270	400
GRV-ITR-12	all	Thermistor: 2252 Curve (°C)	60000021	6000003F	12	°C	-40	150
GRV-ITR-12	all	Thermistor: 3K Curve (°C)	60000021	60000040	12	°C	-40	150

Part number	Applies To	Description	Module ID (hex)	Channel ID (hex)	Channels per module	Default Units	Low Scale	Full Scale
GRV-ITR-12	all	Thermistor: 10K Type 2 Curve (°C)	60000021	60000041	12	°C	-40	150
GRV-ITR-12	all	Thermistor: 10K Type 3 Curve (°C)	60000021	60000042	12	°C	-40	150
GRV-ITR-12	all	Thermistor: Custom Curve (°C)	60000021	60000043	12	°C	-40	150
GRV-ITR-12	all	0–400k Ohms (autorange)	60000021	60000032	12	Ohms	0	400000
GRV-ITR-12	all	0–400k Ohms	60000021	60000033	12	Ohms	0	400000
GRV-ITR-12	all	0–200k Ohms	60000021	60000034	12	Ohms	0	200000
GRV-ITR-12	all	0–100k Ohms	60000021	60000035	12	Ohms	0	100000
GRV-ITR-12	all	0–50k Ohms	60000021	60000036	12	Ohms	0	50000
GRV-ITR-12	all	0–40k Ohms	60000021	60000037	12	Ohms	0	40000
GRV-ITR-12	all	0–20k Ohms	60000021	60000038	12	Ohms	0	20000
GRV-ITR-12	all	0–10k Ohms	60000021	60000039	12	Ohms	0	10000
GRV-ITR-12	all	0–5k Ohms	60000021	6000003A	12	Ohms	0	5000
GRV-ITR-12	all	0–4k Ohms	60000021	6000003B	12	Ohms	0	4000
GRV-ITR-12	all	0–2k Ohms	60000021	6000003C	12	Ohms	0	2000
GRV-ITR-12	all	0–1k Ohms	60000021	6000003D	12	Ohms	0	1000
GRV-ITR-12	all	0–500 Ohms	60000021	6000003E	12	Ohms	0	500
GRV-IV-24	all	±160 V	60000002	60000024	24	V	-160	160
GRV-IV-24	all	±80 V	60000002	6000000D	24	V	-80	80
GRV-IV-24	all	±40 V	60000002	6000000B	24	V	-40	40
GRV-IV-24	all	±20 V	60000002	6000000A	24	V	-20	20
GRV-IV-24	all	±10 V	60000002	60000017	24	V	-10	10
GRV-IV-24	all	±5 V	60000002	60000019	24	V	-5	5
GRV-IV-24	all	±2.5 V	60000002	60000025	24	V	-2.5	2.5
GRV-IV-24	all	±1.25 V	60000002	60000001	24	V	-1.25	1.25
GRV-OAC-12	all	Digital Output	90000012	90000000	12	N/A	N/A	N/A
GRV-OACI-12	all	Digital Output	90000014	90000000	12	N/A	N/A	N/A
GRV-OACIS-12	all	Simple Digital Output	94000017	94000000	12	N/A	N/A	N/A
GRV-OACS-12	all	Simple Digital Output	9400001C	94000000	12	N/A	N/A	N/A
GRV-ODCI-12	all	Digital Output	90000015	90000000	12	N/A	N/A	N/A
GRV-ODCIS-12	all	Simple Digital Output	94000018	94000000	12	N/A	N/A	N/A
GRV-ODCSRC-24	all	Digital Output	90000013	90000000	24	N/A	N/A	N/A
GRV-OMRIS-8	all	Simple Digital Output	94000019	94000000	8	N/A	N/A	N/A
GRV-OVMAILP-8	all	0-20 mA	A0000004	A000001B	8	mA	0	20
GRV-OVMAILP-8	all	0-24 mA	A0000004	A000001C	8	mA	0	24
GRV-OVMAILP-8	all	4-20 mA	A0000004	A000001D	8	mA	4	20
GRV-OVMAILP-8	all	0-10 V	A0000004	A0000020	8	V	0	10
GRV-OVMAILP-8	all	0-5 V	A0000004	A0000022	8	V	0	5
GRV-OVMAILP-8	all	Analog Hi-Z	A0000004	A0000023	8	None	0	0
GRV-OVMALC-8	all	0-20 mA	A0000003	A000001B	8	mA	0	20

Part number	Applies To	Description	Module ID (hex)	Channel ID (hex)	Channels per module	Default Units	Low Scale	Full Scale
GRV-OVMALC-8	all	0-24 mA	A0000003	A000001C	8	mA	0	24
GRV-OVMALC-8	all	4-20 mA	A0000003	A000001D	8	mA	4	20
GRV-OVMALC-8	all	±10 V	A0000003	A000001F	8	V	-10	10
GRV-OVMALC-8	all	0-10 V	A0000003	A0000020	8	V	0	10
GRV-OVMALC-8	all	±5 V	A0000003	A0000021	8	V	-5	5
GRV-OVMALC-8	all	0-5 V	A0000003	A0000022	8	V	0	5
GRV-OVMALC-8	all	Analog Hi-Z	A0000003	A0000023	8	None	0	0

Configuring I/O Channels for *groov* RIO Units

You can configure *groov* RIO units in three ways:

- PAC Control—If you are using PAC Control to create a strategy for your *groov* EPIC or SNAP PAC controller, configure channels there while you are programming your strategy.
- ***groov*** Manage—If your control program is not a PAC Control strategy, or if you are not using a control program, configure channels in *groov* Manage using a web browser on a computer or mobile device. Configurations are automatically saved to flash memory.
- OptoMMP—If OptoMMP is the ONLY communication to the *groov* RIO unit, then configure I/O channels using the configuration values in the following table.

All channels on a *groov* RIO unit use module ID 0xF0000022.

To configure each channel, use the following channel IDs. Make sure the channel you're configuring can use the signal you want.

IMPORTANT: *Thermocouple inputs and discrete sinking outputs cannot be mixed on channels 0–3. To achieve the best thermocouple accuracy when also using current outputs or discrete outputs, always configure thermocouples on the lowest channel numbers and outputs on the highest channel numbers.*

Channels	Function	Signal	Channel ID (hex)	Default units	Low Scale	Full Scale	Overrange
0–1	Discrete DC input with features (see page 169)	5–30 VDC	50000079	VDC	5	30	30
2–7	Simple discrete DC input (on/off state only)	5–30 VDC	5400007A	VDC	5	30	30
0–1	Discrete switch input with features (see page 169)	Switch input, powered	50000068	n/a	n/a	n/a	n/a
2–7	Simple discrete switch input (on/off state only)	Switch input, powered	54000085	n/a	n/a	n/a	n/a
0–7	Discrete DC output, sinking	5–30 VDC	9000007B	VDC	5	30	30
0–7	Analog voltage input	0-10 VDC	60000018	VDC	0	10	11.1
0–7	ICTD (with ICTD probe)	-40 to 100 °C	60000031	Degrees C	-40	100	100
0–3	Analog current input	0–20 mA	60000015	mA	0	20	22.2
0–3	Thermocouple input	Type B	60000009	mV	-75	75	-78 to +78
0–3	Thermocouple input	Type E	6000000C	mV	-75	75	-78 to +78
0–3	Thermocouple input	Type J	6000000E	mV	-75	75	-78 to +78

Channels	Function	Signal	Channel ID (hex)	Default units	Low Scale	Full Scale	Overrange
0–3	Thermocouple input	Type K	6000000F	mV	-75	75	-78 to +78
0–3	Thermocouple input	Type N	60000010	mV	-75	75	-78 to +78
0–3	Thermocouple input	Type R	60000011	mV	-75	75	-78 to +78
0–3	Thermocouple input	Type S	60000012	mV	-75	75	-78 to +78
0–3	Thermocouple input	Type T	60000013	mV	-75	75	-78 to +78
0–3	Analog millivolt input	-150 to +150 mV	60000005	mV	-150	150	166.5
0–3	Analog millivolt input	-75 to +75 mV	60000006	mV	-75	75	83.25
0–3	Analog millivolt input	-25 to +25 mV	60000008	mV	-25	25	27.75
4–7	Analog voltage output	0 to 10 V	A0000020	V	0	10	10
4–7	Analog current output	0 to 20 mA	A000001B	mA	0	20	20
8–9	Mechanical relayoutput	Form C	94000078	n/a	n/a	n/a	n/a

Configuring I/O Channels for SNAP Analog/Digital I/O Units

All SNAP analog/digital I/O units recognize analog, serial, and high-density digital modules on the rack. Positions on the rack that don't contain modules the I/O unit recognizes are assumed to contain digital input modules. If the individual channel types on the module differ from the default type for that module, you must configure the channels.

You can configure SNAP I/O units in three ways:

- PAC Control—If you are using PAC Control, configure channels there while you are programming your strategy.
- PAC Manager—If you are not using PAC Control, configure channels in PAC Manager and save to flash memory.

  CAUTION: *Store to flash only once! Storing to flash memory in a loop can wear out the memory.*

- OptoMMP —If OptoMMP is the ONLY communication to the SNAP I/O unit, then use the values in the SNAP I/O module types and channel types tables (starting on page 21) to configure I/O channels. For SNAP digital-only I/O units, G4EB2s, and E1 and E2 brain boards, see page 29.

About E1 and E2 brain boards: You can configure E1s and E2s like any other I/O unit if you have E1/E2 firmware R1.2a (and higher) and PAC Project 9.5000 (and higher). Also, if a SNAP PAC controller communicates with the E1 or E2, the controller must have PAC firmware R9.5a (or higher) to use this simplified configuration method. If you are not using these firmware and software versions (or if you prefer to use the previous method to reconfigure existing E1s or E2s), see I/O Configuration for E1 an E2 Brain Boards *(form 1576).*

SNAP I/O Module Types and Channel Types

The following tables help you configure channels by showing the part number, the channel type in decimal and in hex, and the module type in hex (module type is read-only). For analog modules, tables also include the number of channels per module, the unit of measurement for the module, and its range. (Some older I/O units cannot use all of these modules; see the module's data sheet for compatibility.)

Default channel types are shaded. If a channel differs from the default, use the value in the Channel Type (Hex) column to configure the channel. For example, if the module in position 0 on the rack is a SNAP-AIV with a -5 to +5 V input, it is not the default for that module. Therefore, you must configure its channels.

As another example, suppose the module in position 1 on the rack is a 4-channel digital output module. Since the default is a 4-channel digital *input* module, you must configure its channels.

In This Section

SNAP Digital Inputs and Outputs

Module & Description	Channel Type (Dec)	Channel Type (Hex)	Module Type (Hex)
4-channel digital input module*	256	100	00
4-channel digital output module*	384	180	00

* High-density digital modules are automatically recognized; channels do not require configuration.

SNAP Analog Inputs

Use this data for configuring channel types (see page 21) and features (see page 31).
If a module has multiple listings, the default channel type is shaded.

Part Number & Description	Channel Type (Dec)	Channel Type (Hex)	Module Type (Hex)	Channels per Module	Default Unit of Measurement	Underrange	Low Scale	Full Scale	Overrange
SNAP-AIARMS: 0–10 A AC/DC	71	47	71	2	A	0.0	0.0	10.0	11.0
SNAP-AIARMS-i: 0–10 A AC/DC	71	47	29	2	A	0.0	0.0	10.0	11.0
SNAP-AIARMS-i-FM: 0–10 A AC/DC	71	47	29	2	A	0.0	0.0	10.0	11.0
SNAP-AICTD: ICTD Temp. Probe	4	4	04	2	Degrees C	-273.0	-40.0	150.0	150.0
SNAP-AICTD-4: ICTD Temp. Probe	4	4	42	4	Degrees C	-273.0	-40.0	150.0	150.0
SNAP-AICTD-8: ICTD Temp. Probe	4	4	4C	8	Degrees C	-273.0	-40.0	150.0	150.0
SNAP-AILC: -2 to +2 mV/V Fast	34	22	0B	2	Percent	-110.0	-100.0	100.0	110.0
SNAP-AILC: -2 to +2 mV/V Slow	36	24	0B	2	Percent	-110.0	-100.0	100.0	110.0
SNAP-AILC: -3 to +3 mV/V Fast	35	23	0B	2	Percent	-110.0	-100.0	100.0	110.0
SNAP-AILC: -3 to +3 mV/V Slow	37	25	0B	2	Percent	-110.0	-100.0	100.0	110.0
SNAP-AILC: Filter of 1st channel	0	0	0B	2	Percent	-110.0	-100.0	100.0	110.0
SNAP-AILC-2: -3 to +3 mV/V Fast	35	23	0C	2	Percent	-110.0	-100.0	100.0	110.0
SNAP-AILC-2: -3 to +3 mV/V Slow	37	25	0C	2	Percent	-110.0	-100.0	100.0	110.0
SNAP-AILC-2: -4 to +4 mV/V Fast	34	22	0C	2	Percent	-110.0	-100.0	100.0	110.0
SNAP-AILC-2: -4 to +4 mV/V Slow	36	24	0C	2	Percent	-110.0	-100.0	100.0	110.0
SNAP-AILC-2: Filter of 1st channel	0	0	0C	2	Percent	-110.0	-100.0	100.0	110.0
SNAP-AIMA: -20 to +20 mA	64	40	64	2	mA	-22.0	-20.0	20.0	22.0
SNAP-AIMA: 0 to +20 mA	2	2	64	2	mA	-22.0	0.0	20.0	22.0
SNAP-AIMA: 4 to +20 mA	3	3	64	2	mA	-22.0	4.0	20.0	22.0
SNAP-AIMA2-i: -1 to +1 mA	85	55	27	2	mA	-1.1	-1.0	1.0	1.1

Part Number & Description	Channel Type (Dec)	Channel Type (Hex)	Module Type (Hex)	Channels per Module	Default Unit of Measurement	Underrange	Low Scale	Full Scale	Overrange
SNAP-AIMA-i: -20 to +20 mA	64	40	22	2	mA	-22.0	-20.0	20.0	22.0
SNAP-AIMA-i: 0 to +20 mA	2	2	22	2	mA	-22.0	0.0	20.0	22.0
SNAP-AIMA-i: 4 to +20 mA	3	3	22	2	mA	-22.0	4.0	20.0	22.0
SNAP-AIMA-iH: 4 to +20 mA	3	3	2A	2	mA	3.2	4.0	20.0	24.0
SNAP-AIMA-iSRC: -20 to +20 mA	64	40	26	2	mA	-22.0	-20.0	20.0	22.0
SNAP-AIMA-iSRC: 0 to +20 mA	2	2	26	2	mA	-22.0	0.0	20.0	22.0
SNAP-AIMA-iSRC: 4 to +20 mA	3	3	26	2	mA	-22.0	4.0	20.0	22.0
SNAP-AIMA-iSRC-FM: -20 to +20 mA	64	40	26	2	mA	-22.0	-20.0	20.0	22.0
SNAP-AIMA-iSRC-FM: 0 to +20 mA	2	2	26	2	mA	-22.0	0.0	20.0	22.0
SNAP-AIMA-iSRC-FM: 4 to +20 mA	3	3	26	2	mA	-22.0	4.0	20.0	22.0
SNAP-AIMA-4: -20 to +20 mA	64	40	40	4	mA	-22.0	-20.0	20.0	22.0
SNAP-AIMA-4: 0 to +20 mA	2	2	40	4	mA	-22.0	0.0	20.0	22.0
SNAP-AIMA-4: 4 to +20 mA	3	3	40	4	mA	-22.0	4.0	20.0	22.0
SNAP-AIMA-8: -20 to +20 mA	64	40	4A	8	mA	-22.0	-20.0	20.0	22.0
SNAP-AIMA-8: 0 to +20 mA	2	2	4A	8	mA	-22.0	0.0	20.0	22.0
SNAP-AIMA-8: 4 to +20 mA	3	3	4A	8	mA	-22.0	4.0	20.0	22.0
SNAP-AIMA-32: -20 to +20 mA	64	40	4D	32	mA	-22.0	-20.0	20.0	22.0
SNAP-AIMA-32: 0 to +20 mA	2	2	4D	32	mA	-22.0	0.0	20.0	22.0
SNAP-AIMA-32: 4 to +20 mA	3	3	4D	32	mA	-22.0	4.0	20.0	22.0
SNAP-AIMA-32-FM: -20 to +20 mA	64	40	4D	32	mA	-22.0	-20.0	20.0	22.0
SNAP-AIMA-32-FM: 0 to +20 mA	2	2	4D	32	mA	-22.0	0.0	20.0	22.0
SNAP-AIMA-32-FM: 4 to +20 mA	3	3	4D	32	mA	-22.0	4.0	20.0	22.0
SNAP-AIMV-4: -150 to +150 mV	66	42	44	4	mV	-165.0	-150.0	150.0	165.0
SNAP-AIMV-4: -75 to +75 mV	68	44	44	4	mV	-82.5	-75.0	75.0	82.5
SNAP-AIMV2-4: -50 to +50 mV	9	9	45	4	mV	-55.0	-50.0	50.0	55.0
SNAP-AIMV2-4: -25 to +25 mV	67	43	45	4	mV	-27.5	-25.0	25.0	27.5
SNAP-AIPM (channel 0 only)	70	46	0A	*	AC VRMS	0.0	0	250	275
SNAP-AIPM (channel 1 only)	71	47	0A	*	AC ARMS	0.0	0	10	11.0
SNAP-AIPM (channel 2 only)	82	52	0A	*	True power	n/a	n/a	n/a	n/a
SNAP-AIPM (channel 3 only)	83	53	0A	*	Volt/Amps	n/a	n/a	n/a	n/a
SNAP-AIPM-3 (channels 0, 4 & 8)	70	46	49	*	AC VRMS	0.0	0	300	330
SNAP-AIPM-3 (channels 1, 5 & 9)	71	47	49	*	AC ARMS	0.0	0	5	5.5
SNAP-AIPM-3 (channels 2, 6 & 10)	82	52	49	*	True power	n/a	n/a	n/a	n/a
SNAP-AIPM-3 (channels 3, 7 & 11)	83	53	49	*	Volt/Amps	n/a	n/a	n/a	n/a
SNAP-AIPM-3 (channels 12 & 13)	86	56	49	*	True power	n/a	n/a	n/a	n/a
SNAP-AIPM-3V (channels 0, 4 & 8)	100	64	48	*	AC VRMS	0.0	0	300	330

Part Number & Description	Channel Type (Dec)	Channel Type (Hex)	Module Type (Hex)	Channels per Module	Default Unit of Measurement	Underrange	Low Scale	Full Scale	Overrange
SNAP-AIPM-3V (channels 1, 5 & 9)	89	59	48	*	VAC from CT	0.0	0	0.333	0.366
SNAP-AIPM-3V (channels 2, 6 & 10)	90	5A	48	*	True power	n/a	n/a	n/a	n/a
SNAP-AIPM-3V (channels 3, 7 & 11)	90	5A	48	*	Volt/Amps	n/a	n/a	n/a	n/a
SNAP-AIPM-3V (channels 12 & 13)	184	B8	48	*	True power	n/a	n/a	n/a	n/a
SNAP-AIRATE: Rate (Frequency)	69	45	69	2	Hz	0.0	0.0	25000.0	27500.0
SNAP-AIRATE-HFi: Rate (0.1 s data freshness)	68	44	2B	2	Hz	2	2	500,000	500,000
SNAP-AIRATE-HFi: Rate (1 s data freshness)	69	45	2B	2	Hz	20	20	500,000	500,000
SNAP-AIRTD: 100 Ohm Pt 3-wire	10	0A	10	2	Degrees C	-200.0	-200.0	850.0	850.0
SNAP-AIRTD: 100 Ohm Ni 3-wire	46	2E	10	2	Degrees C	-60.0	-60.0	250.0	250.0
SNAP-AIRTD: 0–400 Ohms, Lead Compensated	15	0F	10	2	Ohms	0	0	400	440
SNAP-AIRTD: 120 Ohm Ni 3-wire	48	30	10	2	Degrees C	-80.0	-80.0	260.0	260.0
SNAP-AIRTD-10: 10 Ohm Cu 3-wire	14	0E	0E	2	Degrees C	-180.0	-180.0	260.0	260.0
SNAP-AIRTD-10: 0–25 Ohms, Lead Compensated	15	0F	0E	2	Ohms	0	0	25	27.5
SNAP-AIRTD-1K: 1000 Ohm Pt 3-wire	92	5C	0F	2	Degrees C	-200.0	-200.0	850.0	850.0
SNAP-AIRTD-1K: 1000 Ohm Ni 3-wire	93	5D	0F	2	Degrees C	-60.0	-60.0	250.0	250.0
SNAP-AIRTD-1K: 1000 Ohm Ni 3-wire	94	5E	0F	2	Degrees F	-50.0	-50.0	275.0	275.0
SNAP-AIRTD-1K: 0–4000 Ohms, Lead Compensated	15	0F	0F	2	Ohms	0	0	4000	4400
SNAP-AIRTD-8U: 0–8000 Ohms - Fixed	155	9B	55	8	Ohms	0	0	8000	8800
SNAP-AIRTD-8U: 1000 Ohm Ni 3-wire @ 70° F	182	B6	55	8	Degrees F	-46	-46	148.9	148.9
SNAP-AIRTD-8U: 1000 Ohm Ni 3-wire @ 0 °C	181	B5	55	8	Degrees C	-40	-40	135	135
SNAP-AIRTD-8U: 1000 Ohm Pt @ 0 °C	180	B4	55	8	Degrees C	-200	-200	850	850
SNAP-AIRTD-8U: 120 Ohm Ni @ 0 °C	179	B3	55	8	Degrees C	-80	-80	260	260
SNAP-AIRTD-8U: 100 Ohm Ni @ 0 °C	178	B2	55	8	Degrees C	-60	-60	250	250
SNAP-AIRTD-8U: 100 Ohm Pt @ 0 °C	177	B1	55	8	Degrees C	-200	-200	850	850
SNAP-AIRTD-8U: 10 Ohm Cu	176	B0	55	8	Degrees C	-60	-60	355	355
SNAP-AIRTD-8U: 0–8000 Ohms - Auto	171	AB	55	8	Ohms	0	0	8000	8800
SNAP-AIRTD-8U: 0–4000 Ohms - Auto	170	AA	55	8	Ohms	0	0	4000	4400
SNAP-AIRTD-8U: 0–2000 Ohms - Auto	169	A9	55	8	Ohms	0	0	2000	2200
SNAP-AIRTD-8U: 0–1000 Ohms - Auto	168	A8	55	8	Ohms	0	0	1000	1100
SNAP-AIRTD-8U: 0–800 Ohms - Auto	167	A7	55	8	Ohms	0	0	800	880
SNAP-AIRTD-8U: 0–400 Ohms - Auto	166	A6	55	8	Ohms	0	0	400	440
SNAP-AIRTD-8U: 0–200 Ohms - Auto	165	A5	55	8	Ohms	0	0	200	220

Part Number & Description	Channel Type (Dec)	Channel Type (Hex)	Module Type (Hex)	Channels per Module	Default Unit of Measurement	Underrange	Low Scale	Full Scale	Overrange
SNAP-AIRTD-8U: 0–100 Ohms - Auto	164	A4	55	8	Ohms	0	0	100	110
SNAP-AIRTD-8U: 0–80 Ohms - Auto	163	A3	55	8	Ohms	0	0	80	88
SNAP-AIRTD-8U: 0–40 Ohms - Auto	162	A2	55	8	Ohms	0	0	40	44
SNAP-AIRTD-8U: 0–20 Ohms - Auto	161	A1	55	8	Ohms	0	0	20	22
SNAP-AIRTD-8U: 0–10 Ohms - Auto	160	A0	55	8	Ohms	0	0	10	11
SNAP-AIRTD-8U: 0–4000 Ohms - Fixed	154	9A	55	8	Ohms	0	0	4000	4400
SNAP-AIRTD-8U: 0–2000 Ohms - Fixed	153	99	55	8	Ohms	0	0	2000	2200
SNAP-AIRTD-8U: 0–1000 Ohms - Fixed	152	98	55	8	Ohms	0	0	1000	1100
SNAP-AIRTD-8U: 0–800 Ohms - Fixed	151	97	55	8	Ohms	0	0	800	880
SNAP-AIRTD-8U: 0–400 Ohms - Fixed	150	96	55	8	Ohms	0	0	400	440
SNAP-AIRTD-8U: 0–200 Ohms - Fixed	149	95	55	8	Ohms	0	0	200	220
SNAP-AIRTD-8U: 0–100 Ohms - Fixed	148	94	55	8	Ohms	0	0	100	110
SNAP-AIRTD-8U: 0–80 Ohms - Fixed	147	93	55	8	Ohms	0	0	80	88
SNAP-AIRTD-8U: 0–40 Ohms - Fixed	146	92	55	8	Ohms	0	0	40	44
SNAP-AIRTD-8U: 0–20 Ohms - Fixed	145	91	55	8	Ohms	0	0	20	22
SNAP-AIRTD-8U: 0–10 Ohms - Fixed	144	90	55	8	Ohms	0	0	10	11
SNAP-AITM: -150 to +150 mV	66	42	66	2	mV	-165.0	-150.0	150.0	165.0
SNAP-AITM: -75 to +75 mV	68	44	66	2	mV	-82.5	-75.0	75.0	82.5
SNAP-AITM: Type E Thermocouple	19	13	66	2	Degrees C	-270.0	-270.0	1000.0	1000.0
SNAP-AITM: Type J Thermocouple	5	5	66	2	Degrees C	-210.0	-210.0	1200.0	1200.0
SNAP-AITM: Type K Thermocouple	8	8	66	2	Degrees C	-270.0	-270.0	1372.0	1372.0
SNAP-AITM-i: -150 to +150 mV	66	42	20	2	mV	-165.0	-150.0	150.0	165.0
SNAP-AITM-i: -75 to +75 mV	68	44	20	2	mV	-82.5	-75.0	75.0	82.5
SNAP-AITM-i: Type E Thermocouple	19	13	20	2	Degrees C	-270.0	-270.0	1000.0	1000.0
SNAP-AITM-i: Type J Thermocouple	5	5	20	2	Degrees C	-210.0	-210.0	1200.0	1200.0
SNAP-AITM-i: Type K Thermocouple	8	8	20	2	Degrees C	-270.0	-270.0	1372.0	1372.0
SNAP-AITM-4i: -150 to +150 mV	66	42	32	4	mV	-165.0	-150.0	150.0	165.0
SNAP-AITM-4i: -75 to +75 mV	68	44	32	4	mV	-82.5	-75.0	75	82.5
SNAP-AITM-4i: -50 to +50 mV	9	9	32	4	mV	-55.0	-50.0	50.0	55.0
SNAP-AITM-4i: -25 to +25 mV	67	43	32	4	mV	-27.5	-25.0	25.0	27.5
SNAP-AITM-4i: Type B Thermocouple	24	18	32	4	Degrees C	42.0	42.0	1820.0	1820.0
SNAP-AITM-4i: Type C Thermocouple	32	20	32	4	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM-4i: Type D Thermocouple	33	21	32	4	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM-4i: Type E Thermocouple	19	13	32	4	Degrees C	-270.0	-270.0	1000.0	1000.0
SNAP-AITM-4i: Type G Thermocouple	31	1F	32	4	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM-4i: Type J Thermocouple	5	5	32	4	Degrees C	-210.0	-210.0	1200.0	1200.0

Part Number & Description	Channel Type (Dec)	Channel Type (Hex)	Module Type (Hex)	Channels per Module	Default Unit of Measurement	Underrange	Low Scale	Full Scale	Overrange
SNAP-AITM-4i: Type K Thermocouple	8	8	32	4	Degrees C	-270.0	-270.0	1372.0	1372.0
SNAP-AITM-4i: Type N Thermocouple	30	1E	32	4	Degrees C	-270.0	-270.0	1300.0	1300.0
SNAP-AITM-4i: Type R Thermocouple	17	11	32	4	Degrees C	-50.0	-50.0	1768.0	1768.0
SNAP-AITM-4i: Type S Thermocouple	23	17	32	4	Degrees C	-50.0	-50.0	1768.0	1768.0
SNAP-AITM-4i: Type T Thermocouple	18	12	32	4	Degrees C	-270.0	-270.0	400.0	400.0
SNAP-AITM-8: -75 to +75 mV	68	44	4F	8	mV	-82.5	-75.0	75.0	82.5
SNAP-AITM-8: -50 to +50 mV	9	9	4F	8	mV	-55.0	-50.0	50.0	55.0
SNAP-AITM-8: -25 to +25 mV	67	43	4F	8	mV	-27.5	-25.0	25.0	27.5
SNAP-AITM-8: Type B Thermocouple	24	18	4F	8	Degrees C	42.0	42.0	1820.0	1820.0
SNAP-AITM-8: Type C Thermocouple	32	20	4F	8	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM-8: Type D Thermocouple	33	21	4F	8	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM-8: Type E Thermocouple	19	13	4F	8	Degrees C	-270.0	-270.0	1000.0	1000.0
SNAP-AITM-8: Type G Thermocouple	31	1F	4F	8	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM-8: Type J Thermocouple	5	5	4F	8	Degrees C	-210.0	-210.0	1200.0	1200.0
SNAP-AITM-8: Type K Thermocouple	8	8	4F	8	Degrees C	-270.0	-270.0	1372.0	1372.0
SNAP-AITM-8: Type N Thermocouple	30	1E	4F	8	Degrees C	-270.0	-270.0	1300.0	1300.0
SNAP-AITM-8: Type R Thermocouple	17	11	4F	8	Degrees C	-50.0	-50.0	1768.0	1768.0
SNAP-AITM-8: Type S Thermocouple	23	17	4F	8	Degrees C	-50.0	-50.0	1768.0	1768.0
SNAP-AITM-8: Type T Thermocouple	18	12	4F	8	Degrees C	-270.0	-270.0	400.0	400.0
SNAP-AITM-8-FM: -75 to +75 mV	68	44	4F	8	mV	-82.5	-75.0	75.0	82.5
SNAP-AITM-8-FM: -50 to +50 mV	9	9	4F	8	mV	-55.0	-50.0	50.0	55.0
SNAP-AITM-8-FM: -25 to +25 mV	67	43	4F	8	mV	-27.5	-25.0	25.0	27.5
SNAP-AITM-8-FM: Type B Thermocouple	24	18	4F	8	Degrees C	42.0	42.0	1820.0	1820.0
SNAP-AITM-8-FM: Type C Thermocouple	32	20	4F	8	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM-8-FM: Type D Thermocouple	33	21	4F	8	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM-8-FM: Type E Thermocouple	19	13	4F	8	Degrees C	-270.0	-270.0	1000.0	1000.0
SNAP-AITM-8-FM: Type G Thermocouple	31	1F	4F	8	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM-8-FM: Type J Thermocouple	5	5	4F	8	Degrees C	-210.0	-210.0	1200.0	1200.0
SNAP-AITM-8-FM: Type K Thermocouple	8	8	4F	8	Degrees C	-270.0	-270.0	1372.0	1372.0
SNAP-AITM-8-FM: Type N Thermocouple	30	1E	4F	8	Degrees C	-270.0	-270.0	1300.0	1300.0
SNAP-AITM-8-FM: Type R Thermocouple	17	11	4F	8	Degrees C	-50.0	-50.0	1768.0	1768.0
SNAP-AITM-8-FM: Type S Thermocouple	23	17	4F	8	Degrees C	-50.0	-50.0	1768.0	1768.0
SNAP-AITM-8-FM: Type T Thermocouple	18	12	4F	8	Degrees C	-270.0	-270.0	400.0	400.0
SNAP-AITM2: -50 to +50 mV	9	9	09	2	mV	-55.0	-50.0	50.0	55.0
SNAP-AITM2: -25 to +25 mV	67	43	09	2	mV	-27.5	-25.0	25.0	27.5
SNAP-AITM2: Type B Thermocouple	24	18	09	2	Degrees C	42.0	42.0	1820.0	1820.0

Part Number & Description	Channel Type (Dec)	Channel Type (Hex)	Module Type (Hex)	Channels per Module	Default Unit of Measurement	Underrange	Low Scale	Full Scale	Overrange
SNAP-AITM2: Type C Thermocouple	32	20	09	2	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM2: Type D Thermocouple	33	21	09	2	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM2: Type G Thermocouple	31	1F	09	2	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM2: Type N Thermocouple	30	1E	09	2	Degrees C	-270.0	-270.0	1300.0	1300.0
SNAP-AITM2: Type R Thermocouple	17	11	09	2	Degrees C	-50.0	-50.0	1768.0	1768.0
SNAP-AITM2: Type S Thermocouple	23	17	09	2	Degrees C	-50.0	-50.0	1768.0	1768.0
SNAP-AITM2: Type T Thermocouple	18	12	09	2	Degrees C	-270.0	-270.0	400.0	400.0
SNAP-AITM2-i: -50 to +50 mV	9	9	21	2	mV	-55.0	-50.0	50.0	55.0
SNAP-AITM2-i: -25 to +25 mV	67	43	21	2	mV	-27.5	-25.0	25.0	27.5
SNAP-AITM2-i: Type B Thermocouple	24	18	21	2	Degrees C	42.0	42.0	1820.0	1820.0
SNAP-AITM2-i: Type C Thermocouple	32	20	21	2	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM2-i: Type D Thermocouple	33	21	21	2	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM2-i: Type G Thermocouple	31	1F	21	2	Degrees C	0.0	0.0	2320.0	2320.0
SNAP-AITM2-i: Type N Thermocouple	30	1E	21	2	Degrees C	-270.0	-270.0	1300.0	1300.0
SNAP-AITM2-i: Type R Thermocouple	17	11	21	2	Degrees C	-50.0	-50.0	1768.0	1768.0
SNAP-AITM2-i: Type S Thermocouple	23	17	21	2	Degrees C	-50.0	-50.0	1768.0	1768.0
SNAP-AITM2-i: Type T Thermocouple	18	12	21	2	Degrees C	-270.0	-270.0	400.0	400.0
SNAP-AIV: -10 to +10 VDC	12	C	12	2	VDC	-11.0	-10.0	10.0	11.0
SNAP-AIV: -5 to +5 VDC	11	B	12	2	VDC	-5.5	-5.0	5.0	5.5
SNAP-AIV-i: -10 to +10 VDC	12	C	23	2	VDC	-11.0	-10.0	10.0	11.0
SNAP-AIV-i: -5 to +5 VDC	11	B	23	2	VDC	-5.5	-5.0	5.0	5.5
SNAP-AIV-4: -10 to +10 VDC	12	C	41	4	VDC	-11.0	-10.0	10.0	11.0
SNAP-AIV-4: -5 to +5 VDC	11	B	41	4	VDC	-5.5	-5.0	5.0	5.5
SNAP-AIV-8: -10 to +10 VDC	12	C	4B	8	VDC	-11.0	-10.0	10.0	11.0
SNAP-AIV-8: -5 to +5 VDC	11	B	4B	8	VDC	-5.5	-5.0	5.0	5.5
SNAP-AIV-32: -10 to +10 VDC	12	C	4E	32	VDC	-11.0	-10.0	10.0	11.0
SNAP-AIV-32: -5 to +5 VDC	11	B	4E	32	VDC	-5.5	-5.0	5.0	5.5
SNAP-AIV-32-FM: -10 to +10 VDC	12	C	4E	32	VDC	-11.0	-10.0	10.0	11.0
SNAP-AIV-32-FM: -5 to +5 VDC	11	B	4E	32	VDC	-5.5	-5.0	5.0	5.5
SNAP-AIV2-i: -100 to +100 VDC	72	48	24	2	VDC	-110.0	-100.0	100.0	110.0
SNAP-AIV2-i: -50 to +50 VDC	73	49	24	2	VDC	-55.0	-50.0	50.0	55.0
SNAP-AIVRMS: 0–250 VAC/VDC	70	46	70	2	VAC/VDC	0.0	0.0	250.0	275.0
SNAP-AIVRMS-i: 0–250 VAC/VDC	70	46	28	2	VAC/VDC	0.0	0.0	250.0	275.0
SNAP-AIVRMS-i-FM: 0–250 VAC/VDC	70	46	28	2	VAC/VDC	0.0	0.0	250.0	275.0
SNAP-AIR40K-4: 0 to 40K Ohms	74	4A	43	4	Ohms	0	0	40,000	44,000
SNAP-AIR40K-4: 0 to 20K Ohms	75	4B	43	4	Ohms	0	0	20,000	22,000

Part Number & Description	Channel Type (Dec)	Channel Type (Hex)	Module Type (Hex)	Channels per Module	Default Unit of Measurement	Underrange	Low Scale	Full Scale	Overrange
SNAP-AIR40K-4: 0 to 10K Ohms	76	4C	43	4	Ohms	0	0	10,000	11,000
SNAP-AIR40K-4: 0 to 5K Ohms	77	4D	43	4	Ohms	0	0	5000	5500
SNAP-AIR400K-8: 0 to 400K Ohms	105	69	54	8	Ohms	0	0	400,000	440,000
SNAP-AIR400K-8: 0 to 400K Autorange	188	BC	54	8	Ohms	0	0	400,000	440,000
SNAP-AIR400K-8: 0 to 200K Ohms	106	6A	54	8	Ohms	0	0	200,000	220,000
SNAP-AIR400K-8: 0 to 100K Ohms	107	6B	54	8	Ohms	0	0	100,000	110,000
SNAP-AIR400K-8: 0 to 50K Ohms	108	6C	54	8	Ohms	0	0	50,000	55,000
SNAP-AIR400K-8: 0 to 40K Ohms	74	4A	54	8	Ohms	0	0	40,000	44,000
SNAP-AIR400K-8: 0 to 20K Ohms	75	4B	54	8	Ohms	0	0	20,000	22,000
SNAP-AIR400K-8: 0 to 10K Ohms	76	4C	54	8	Ohms	0	0	10,000	11,000
SNAP-AIR400K-8: 0 to 5K Ohms	77	4D	54	8	Ohms	0	0	5000	5500
SNAP-AIR400K-8: 0 to 4K Ohms	38	26	54	8	Ohms	0	0	4000	4400
SNAP-AIR400K-8: 0 to 2K Ohms	39	27	54	8	Ohms	0	0	2000	2200
SNAP-AIR400K-8: 0 to 1K Ohms	40	28	54	8	Ohms	0	0	1000	1100
SNAP-AIR400K-8: 0 to 500 Ohms	41	29	54	8	Ohms	0	0	500	550
SNAP-pH/ORP: -1 to +1 VDC	78	4E	25	2	VDC	-1.1	-1.0	1.0	1.1
SNAP-pH/ORP: 0–14 pH	79	4F	25	2	pH	-1.4	0.0	14.0	15.4
SNAP-pH/ORP: -0.5 to +0.5 VDC	80	50	25	2	VDC	-0.55	-0.5	0.5	0.55
SNAP-PID-V	99	63	D0	4	Percent	0	0	100.0	110.0

* The SNAP-AIPM module monitors one device from channel 0 (volts) and channel 1 (amps). Channels 2 and 3 return calculated values. The SNAP-AIPM-3 and SNAP-AIPM-3V monitor three phases from channels 0,4, & 8 (volts) and channels 1,5, & 9 (amps). All other channels return calculated values. See the *SNAP AIPM Modules Data Sheet* (form 1453) for details.

SNAP Analog Outputs

Use this data for configuring channel types (see page 21) and features (see page 31).
If a module has multiple listings, the default channel type is shaded.

Part Number & Description	Channel Type (Dec)	Channel Type (Hex)	Module Type (Hex)	Channels per Module	Default Unit of Measurement	Underrange	Low scale	Full scale	Overrange
SNAP-AOA-3: 4–20 mA	131	83	83	1	mA	4.0	4.0	20.0	20.0
SNAP-AOV-5: 0–10 VDC	133	85	85	1	VDC	0.0	0.0	10.0	10.0
SNAP-AOA-23: 4–20 mA	163	A3	A3	2	mA	4.0	4.0	20.0	20.0
SNAP-AOA-23-iSRC: 4–20 mA	163	A3	B3	2	mA	4.0	4.0	20.0	20.0

Part Number & Description	Channel Type (Dec)	Channel Type (Hex)	Module Type (Hex)	Channels per Module	Default Unit of Measurement	Underrange	Low scale	Full scale	Overrange
SNAP-AOA-23-iSRC-FM: 4–20 mA	163	A3	B3	2	mA	4.0	4.0	20.0	20.0
SNAP-AOA-23-iH: 4–20 mA	163	A3	AB	2	mA	4.0	4.0	20.0	20.0
SNAP-AOV-25: 0–10 VDC	165	A5	A5	2	VDC	0.0	0.0	10.0	10.0
SNAP-AOV-27: -10 to +10 VDC	167	A7	A7	2	VDC	-10.0	-10.0	10.0	10.0
SNAP-AOA-28: 0–20 mA	168	A8	A8	2	mA	0.0	0.0	20.0	20.0
SNAP-AOVA-8: 0–5 VDC	144	90	CF	8	VDC	0.0	0.0	5.0	5.0
SNAP-AOVA-8: 0–10 VDC	145	91	CF	8	VDC	0.0	0.0	10.0	10.0
SNAP-AOVA-8: -5 to +5 VDC	146	92	CF	8	VDC	-5.0	-5.0	5.0	5.0
SNAP-AOVA-8: -10 to +10 VDC	147	93	CF	8	VDC	-10.0	-10.0	10.0	10.0
SNAP-AOVA-8: 4–20 mA	148	94	CF	8	mA	4.0	4.0	20.0	20.0
SNAP-AOVA-8: 0–20 mA	149	95	CF	8	mA	0.0	0.0	20.0	20.0
SNAP-AOD-29: TPO 5–60 VDC	169	A9	A9	2	Percent	n/a	0.0	100.0	n/a
SNAP-AOD-29-HFi: TPO 2.5–24 VDC	131	83	B9	2	Percent	n/a	0.0	100.0	n/a

UIO
EIO
G4EB2

Digital-only SNAP and G4EB2 I/O units. The digital-only SNAP-UP1-D64 and SNAP-ENET-D64 I/O units assume that all positions on the rack contain 4-channel digital input modules. If a position contains an output module, you must configure its channels as outputs (using the channel type 180).

See "(Expanded) Analog & Digital Channel Configuration—Read/Write" on page 85.

E1
E2

E1 and E2 brain boards. The method for configuring E1 and E2 brain boards was simplified in PAC Manager R9.5a and E1/E2 firmware R1.2a. Newer installations should use the new method, but you don't need to change any I/O unit that's already configured. You can still use the earlier method (documented in I/O *Configuration for E1 and E2 Brain Boards*, form 1576) for changes to existing I/O units.

Before trying to read or write to channels, use PAC Manager R9.5a (or higher) or the "(Expanded) Analog & Digital Channel Configuration—Read/Write" on page 85 area to configure channel types and features for all channels on the rack.

E1—If the E1 has firmware R1.2a or higher, the channel type defaults to 0x100, which indicates a digital input. For an output, change the channel type to 0x180.

If your E1 has firmware lower than R1.2a, the channel type defaults to 0x00. Write 0x100 for an input or 0x180 for an output.

E2—To use the new simplified configuration method, upgrade E2 firmware to version R1.2a or higher. The new method uses new module/channel types for the G1 modules on the E2 rack. See "Analog Channel Type Configuration Table (E2)" on page 30.

IMPORTANT: *E2 I/O unit modules configured with the new method will report Engineering units as G1 counts (0 to +4095 nominal range). Modules configured with the old method (from form 1576) will report Engineering units as SNAP counts (0 to +25000, or -25000 to +25000).*

E2

Analog Channel Type Configuration Table (E2)

The method for configuring E1 and E2 brain boards was simplified in PAC Manager R9.5a and E1/E2 firmware R1.2a (see details on page 21), so you can now configure E1s and E2s in the same way you would SNAP PAC brains.

IMPORTANT: *E2 I/O unit modules configured with the new method will report Engineering units as G1 counts (0 to +4095 nominal range). Modules configured with the old method (described in form 1576) will report Engineering units as SNAP counts (0 to +25000, or -25000 to +25000).*

The new method uses new module/channel types for the G1 modules on the E2 rack.

The following table shows the module part number, the channel type to write, and the equivalent old method if you need to change methods on an existing I/O unit (not required).

Module Part Number	New method Module/ Channel Type	Range and Units	Old method SNAP I/O Channel Type Equivalents
AD2T	0x202	0–20 mA	0x40 (SNAP-AIMA: -20 to +20 mA)
AD3	0x203	4–20 mA	0x22 (SNAP-CUSTOM-AI: Mode 1)
AD4	0x204	ICTD Temp. Probe	0x04 (SNAP-AICTD: ICTD Temp. Probe)
AD5	0x205	Type J Thermocouple	0x05 (SNAP-AITM: Type J Thermocouple)
AD6	0x206	0–5 VDC	0x49 (SNAP-AIV2-i: -50 to +50 VDC)
AD7	0x207	0–10 VDC	0x48 (SNAP-AIV2-i: -100 to +100 VDC)
AD8	0x208	Type K Thermocouple	0x08 (SNAP-AITM: Type K Thermocouple)
AD9T	0x209	0–50 mV	0x09 (SNAP-AITM2-i: -50 to +50 mV)
AD10T2	0x20A	100 Ohm RTD	0x0A (SNAP-AIRTD: 100 Ohm Pt 3-wire)
AD11	0x20B	-5 to +5 VDC	0x0B (SNAP-AIV: -5 to +5 VDC)
AD12	0x20C	-10 to +10 VDC	0x0C (SNAP-AIV: -10 to +10 VDC)
AD13T	0x20D	0–100 mV	0x42 (SNAP-AITM: -150 to +150 mV)
AD14T	0x20E	10 Ohm RTD	0x30 (SNAP-AIRTD: 120 Ohm Ni 3-wire)
AD15T	0x20F	28–140 VAC	0x46 (SNAP-AIVRMS: 0 to 250 VAC/VDC)
AD16T	0x210	0–5 A AC/DC	0x47 (SNAP-AIARMS: 0 to 10 A AC/DC)
AD17T	0x211	Type R Thermocouple	0x11 (SNAP-AITM2: Type R Thermocouple)
AD18T	0x212	Type T Thermocouple	0x12 (SNAP-AITM2: Type T Thermocouple)
AD19T	0x213	Type E Thermocouple	0x13 (SNAP-AITM: Type E Thermocouple)
AD20	0x214	Rate (Frequency)	0x45 (SNAP-AIRATE: Rate - Frequency)
AD17T	0x217	Type S Thermocouple	0x17 (SNAP-AITM2: Type S Thermocouple)
DA3(T)	0x283	4–20 mA	0x83 (SNAP-AOA-3: 4 to 20 mA)
DA4(T)	0x284	0–5 VDC	0xA5 (SNAP-AOV-25: 0 to 10 VDC)
DA5	0x285	0–10 VDC	0x85 (SNAP-AOV-5: 0 to 10 VDC)
DA6	0x286	-5 to +5 VDC	0xA7 (SNAP-AOV-27: -10 to +10 VDC)
DA7	0x287	-10 to +10 VDC	0x87 (SNAP-AOV-7: -10 to +10 VDC)
DA8	0x288	0–20 mA	0xA8 (SNAP-AOA-28: 0 to 20 mA)

CONFIGURING CHANNEL FEATURES

PR1
RIO
PAC-R
EB
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SIO
E1
E2
G4EB2

Channel features vary based on the I/O processor (brain, brain board, or on-the-rack controller or processor) and the module. A few channel features are not accessible through the OptoMMP memory map and can only be used with PAC Control commands; these include analog ramping and analog totalizing.

NOTE: This section uses the terms "digital" and "discrete" interchangeably.

The following channel features are not automatic and must be configured for each channel that uses them:

- Digital input counters and quadrature counters (Exception: Counters on high-density digital modules are automatic and don't need configuring unless you are using PAC Control.)
- Digital and analog watchdogs
- Analog scaling, clamping, offset and gain, and average filter weight

Selecting Configuration Values for I/O Channel Features

NOTE: groov I/O and groov RIO do not include 4-channel digital modules. They are considered to be high-density digital.

Some channels on groov RIO are "simple" discrete channels that support only on/off state and no other features (see "groov RIO Features" on page 169). Similarly, the following groov "simple" discrete I/O modules support state only and no other digital features.

- GRV-IACDCTTLS-24
- GRV-IACHVS-24
- GRV-IACIHVS-12
- GRV-IACS-24
- GRV-IDCIS-12
- GRV-IDCS-24
- GRV-OACIS-12
- GRV-OACS-12
- GRV-ODCIS-12
- GRV-OMRIS-8

The I/O channel features available on I/O units depend on the combined capabilities of the I/O processor, the module, and in some cases, the protocol used. To determine which features are available for the devices you are using, see:

- Appendix C: SNAP Features Comparison Chart
- Appendix D: groov EPIC and groov RIO Features and Comparison Charts.

For more information on using them in your application, see the referenced pages.

Feature	Description	See
State	(digital inputs and outputs)—A digital channel is either on or off. You can read the current state of a digital input or write an on/off state to a digital output.	page 32
Latches	(digital inputs)—When the value of a digital input channel changes from off to on, an on-latch is automatically set. While the value of the channel may return to off, the on-latch remains set, as a record of the change, until you clear it. Similarly, an off-latch is set when the value of a digital channel changes from on to off, and it remains set until cleared.	page 33
Counters	(digital inputs)—A counter keeps track of the number of times a digital input changes from off to on. The count accumulates until it reaches the maximum count available in the I/O unit or until you reset the counter to zero. For example, to count the number of widgets produced per shift, you would clear the counter at the start of each shift and read it at the end of each shift. The speed of the counter depends upon the I/O processor's capabilities and the speed of the module used.	page 33
Quadrature counters	(digital input)—A quadrature counter requires a SNAP quadrature input module, which is attached to the encoder device. The module sends a pulse to the I/O unit upon each change in quadrature state, and the I/O unit counts the pulses and keeps track of the direction and rotation.	page 34

Feature	Description	See
Frequency measurement	(digital input)—Frequency is the speed with which a digital channel changes state and is usually measured in counts per second. For example, reading the frequency can help you determine the speed of rotating machinery. Frequency measurement can be one-time or continuous.	page 35
Period measurement	(digital input)—Period refers to the elapsed time for a complete on-off-on transition on a digital channel. Measurement starts on the first transition (either off-to-on or on-to-off) and stops on the next transition of the same type. Period measurement can be one-time or continuous.	page 35
Pulse measurement	(digital input)—Measures the duration of a pulse, either an on-pulse or an off-pulse.	page 34
Digital Totalizer	(digital input)—A digital totalizer accumulates the total amount of time that a digital input is on (or off). The on-time totalizer shows how long the channel has been on; the off-time totalizer shows how long the channel has been off. Totalizers are often used to determine maintenance or use schedules.	page 35
Watchdog	(digital and analog channels)—A watchdog monitors communication on the OptoMMP port (port 2001, unless you have changed it). If nothing accesses the port for the length of time set in the watchdog, the I/O unit automatically sets designated digital and analog I/O channels to the values you have determined. A watchdog helps make sure that a communication failure doesn't result in disaster. If communication fails between the host and the I/O unit controlling a process, the watchdog makes sure the process is automatically brought to a safe state. For example, a valve could automatically close to avoid completely emptying a tank.	page 36
Scaling	(analog channels)—Analog input and output channels can be scaled as needed. For example, you can scale a -5 V to +5 V input channel to reflect 0% to 100%	page 36
Minimum and maximum values	(analog inputs)—Minimum and maximum values are sometimes called peaks and valleys. You can read these values at any time, for example, to record minimum and maximum temperatures. You can also reset min/max values. For example, if you want to record the maximum temperature at channel 2 in each 24-hour period, you must reset the values after they are read each day.	page 37
Offset and gain	(analog inputs) Offset and gain calculations are used to calibrate analog channels. If a -50 mV to +50 mV input receives signals that are slightly off (not exactly -50 mV at the lowest channel, for example), the offset and gain can be calculated so that values will appear accurately when read.	page 37
Clamping	(analog outputs)—Clamping limits values that can be sent to analog output channels so they do not go above or below a specific value. For example, if you are using a 0–10 VDC output module, but the device attached to one of its channels can only handle a maximum of 5 VDC, you can set an upper clamp of 5 VDC for that channel. The values for upper and lower clamp are set in engineering units.	page 37
Average filter weight	(analog inputs)—A filter weight smooths analog input signals that are erratic or change suddenly.	page 37

PR1
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SIO
E1
G4EB2

States (Digital Channels)

You can read the ON or OFF state of a digital input channel or write to a digital output channel to turn it on or off. This feature is automatic and needs no configuration.

For E1 brain boards, each channel on the unit is treated like the first channel on a SNAP module; that is, only the first of every four channels contains data. For more information on interpreting data formats, see page 58.

PR1
RIO
PAC-R
EB
SB
UIO
EIO
SIO
E1
G4EB2

Latches (Digital Channels)

PR1, RIO—Does not apply to *groov* simple I/O modules or *groov* RIO simple discrete channels. For details, see NOTE on page 31.

SNAP, and G4EB2—Latching is available on single-channel, 4-channel, and high-density digital channels. It is automatic and needs no configuration. Using memory map values, you can read the on-latch or off-latch state of a digital channel, and you can clear latches.

E1—Latching is available on all modules used with the E1. Note that latching is different on an E1 depending on the protocol used with the brain board. When the E1 is used with the Optomux protocol, only one latch is available and you must configure it to be an on-to-off latch or an off-to-on latch. When you use an E1 with PAC Control or OptoMMP, however, both types of latches are automatically available for each channel, and no configuration is required.

To read and/or clear latches, remember that each channel on an E1 is treated like the first channel on a SNAP module, and each channel on a G4EB2 falls within the first four channels of a SNAP module. For example, to read latches for E1 or G4EB2 channels using the Digital Channel Read area of the memory map, read the following addresses:

This module position on E1:	0	1	2	3
Or this channel on G4EB2:	0	4	8	12
Is like this module,channel on SNAP:	0,0	1,0	2,0	3,0
Address for on-latch state:	F080 0004	F080 0104	F080 0204	F080 0304
Address for off-latch state:	F080 0008	F080 0108	F080 0208	F080 0308

PR1
RIO
PAC-R
EB
SB
UIO
EIO
SIO
E1
G4EB2

Counters (Digital Channels)

PR1, RIO—Does not apply to *groov* simple I/O modules or *groov* RIO simple discrete channels. For details, see NOTE on page 31.

SNAP—Any SNAP digital input can be used as a counter. Note the differences in counting between 4-channel and high-density digital modules:

	SNAP 4-channel digital counters	SNAP high-density digital counters
Processor compatibility	SNAP-PAC-R1 (-FM, -W) SNAP-PAC-EB1 (-FM, -W) SNAP-PAC-SB1 SNAP-B3000-ENET SNAP-ENET-RTC SNAP-UP1-ADS	SNAP-PAC-R1 (-FM, -W) SNAP-PAC-R2 (-FM, -W) SNAP-PAC-EB1 (-FM, -W) SNAP-PAC-EB2 (-FM, -W) SNAP-PAC-SB1 SNAP-PAC-SB2 SNAP-B3000-ENET SNAP-ENET-RTC SNAP-ENET-S64 SNAP-UP1-ADS SNAP-UP1-M64
Counting is done on...	**...the brain**	**...the module**
Counting speed	High speed (depends on speed of module; modules available up to 20 KHz)	Low speed (up to 50 Hz)
Configuration and Use	• Each channel to be used as a counter must be configured. • Counters start as soon as configured. • Counters can be Started, Stopped, Read, and Read & Cleared.	• Configure channels only if using PAC Control. • Counters are always counting. • Counters can be Read or Read & Cleared. • Counters cannot be Started or Stopped.

G4EB2—Any digital input can be used as a counter. Counters must be configured. They start as soon as they are configured and can be Started, Stopped, Read, and Read & Cleared.

E1—Any digital input can be used as a counter. Counters must be configured, either in PAC Manager or in your custom application.

Use memory map values in the Channel Configuration area to work with counters.

PR1
PAC-R
EB
SB
UIO
EIO

Quadrature Counters (Digital Inputs)

PR1—Does not apply to *groov* simple I/O modules. For details, see NOTE on page 31.

SNAP—I/O units with the following SNAP I/O processors support quadrature counters for quadrature encoder devices:

- SNAP-PAC-R1
- SNAP-PAC-EB1
- SNAP-PAC-SB1
- SNAP-UP1-ADS
- SNAP-B3000-ENET
- SNAP-ENET-RTC

In SNAP I/O units, a quadrature counter requires a SNAP quadrature input module (SNAP-IDC5Q), which is attached to the encoder device. The module sends a pulse to the processor upon each change in quadrature state, and the processor counts the pulses and keeps track of the direction and rotation. For each axis, the counter counts up if Phase A leads Phase B; it counts down if Phase A lags behind Phase B. Each axis can have counts from 0 to 2,147,483,647.

If your encoder device has an index feature, you can use two separate digital input channels as indexes, one for each axis. The index automatically resets the count, and it shows what the count was when the index was triggered. Counts are sometimes lost, due to noise or encoder problems, for example; with the index, you can see whether the count varies too much.

See the *Using Quadrature Counters* technical note (form 1823), for details on programming quadrature counters.

PR1
RIO
PAC-R
EB
SB
UIO
EIO
E1
G4EB2

Pulse Measurement (Digital Inputs)

PR1, RIO—Does not apply to *groov* simple I/O modules or *groov* RIO simple discrete channels. For details, see NOTE on page 31.

You can measure the duration of a pulse on any digital input. Pulse measurement must be configured by writing to the Channel Feature memory map address as follows (for example, for module 0 channel 0, you would write one of these values to address F010 0008):

- On-pulse: 0x00000009
- Off-pulse: 0x0000000A

Measurement begins at the next leading edge and ends at the following trailing edge. When the measurement is complete, the feature number is cleared, the counter stops, and a completion bit is set for the channel (for example, for module 0 channel 0, in address F040 0024). When the Channel Feature is reset, the completion bit is cleared.

Read the pulse measurement in the Feature Value field (see "Digital Channel Read—Read Only" on page 121)—for example, for module 0 channel 0, in address F080 0010. This value is a 32-bit unsigned integer. Units and resolution are in increments of 100 microseconds (0.1 msec or 0.0001 seconds). For example, a 60 Hz frequency can be counted with a resolution of 166.6, which is calculated as follows:

```
Resolution = 1/(Frequency * Resolution) = 1/(60 * 0.0001) = 166.6
```

PR1
RIO
PAC-R
EB
SB
UIO
EIO
E1
G4EB2

Frequency or Period Measurement (Digital Inputs)

PR1, RIO—Does not apply to *groov* simple I/O modules or *groov* RIO simple discrete channels. For details, see NOTE on page 31.

You can measure frequency or period, either one-time or continuously, on digital inputs. You must configure frequency or period measurement for each channel.

After you've configured the channel feature, you can read the frequency or period measurement in the Feature Value field (see "Digital Channel Read—Read Only" on page 121)—for example, for module 0 channel 0, in address F080 0010. This value is a 32-bit unsigned integer. Units and resolution are in increments of 100 microseconds. For example, a 60 Hz frequency can be counted with a resolution of 166.6, which is calculated as follows:

```
Resolution = 1/(Frequency * Resolution) = 1/(60 * 0.0001) = 166.6
```

One-Time Measurement

Write to the Channel Feature memory map address as follows (for example, for module 0 channel 0, you would write one of these values to address F010 0008):

- For one-time period measurement: 0x0000000B
- For one-time frequency measurement: 0x0000000C

When the measurement is complete, the feature number is cleared, the counter stops, and a completion bit is set for the channel (for example, for module 0 channel 0, in address F040 0024). When the Channel Feature is reset, the completion bit is cleared.

Continuous Measurement

Write to the Channel Feature memory map address as follows (for example, for module 0 channel 0, you would write one of these values to address F010 0008):

- For continuous period measurement: 0x00000003
- For continuous frequency measurement: 0x00000005

PR1
RIO
PAC-R
EB
SB
UIO
EIO
E1
G4EB2

Digital Totalizer

PR1, RIO—Does not apply to *groov* simple I/O modules or *groov* RIO simple discrete channels. For details, see NOTE on page 31.

A digital totalizer can be configured for any digital channel (exception: totalizing is not available on *groov* RIO discrete outputs). Write to the Channel Feature memory map address as follows (for example, for module 0 channel 0, you would write one of these values to address F010 0008):

- For on-time totalizer: 0x00000002
- For off-time totalizer: 0x00000012

Read the totalizer value in the Feature Value field (see "Digital Channel Read—Read Only" on page 121)—for example, for module 0 channel 0, in address F080 0010.

PR1
RIO
PAC-R
EB
SB
UIO
EIO
SIO
E1
E2
G4EB2

Watchdog (Digital and Analog Channels)

PR1, RIO—Does not apply to *groov* simple I/O modules or *groov* RIO simple discrete channels. For details, see NOTE on page 31.

To configure a watchdog, set the watchdog when configuring the *I/O unit*. Then when you configure a digital or analog output channel, you can choose the status or value the channel should be set to if the watchdog timer expires.

Some older SNAP I/O units do not include watchdogs on high-density digital channels. For details, see Appendix C: SNAP Features Comparison Chart.

PR1
RIO
PAC-R
EB
SB
UIO
EIO
SIO
E2

Scaling (Analog Channels)

You can scale analog input or output channels to match your needs. For example, you can scale a -5 V to +5 V input channel to reflect 0% to 100%. Channel types may be unipolar or bipolar.

Examples of Unipolar Channels	Examples of Bipolar Channels
4–20 mA analog output	-25 mV to +25 mV analog input
0–10 A RMS analog input	-10 to +10 VDC analog output

Unipolar and bipolar channels are scaled in the same way, with the lowest reading reflecting the low scale and the highest reading reflecting the high scale. Here are two examples:

	Unipolar Input Channel		**Bipolar Input Channel**		
	Low scale	High scale	Low scale		High scale
Actual reading	0 mA	20 mA	-5 V	0 V	+5 V
Scaled for percentage	0%	100%	0%	50%	100%
Scaled for counts*	0	+25,000	-25,000	0	+25,000

*Counts for input channels always range -25,000 to +25,000.

	Unipolar Output Channel		**Bipolar Output Channel**		
	Low scale	High scale	Low scale		High scale
Actual reading	4 mA	20 mA	-10 VDC	0 VDC	+10 VDC
Scaled for percentage	0%	100%	0%	50%	100%
Scaled for counts*	0	4,095	0	2,047.5	4,095

*Counts for output channels always range 0–4,095.

NOTE: With SNAP PAC firmware version R8.1 and higher, you can also use inverted scaling with analog input channels; however, inverted scaling is not supported with analog output channels. Here's an example of inverted scaling:

0 mA	*20 mA*
742 fpm	*-27 fpm*

To scale an analog channel, see the instructions in the *PAC Manager User's Guide* (form 1704).

PR1
RIO
PAC-R
EB
SB
UIO
EIO
SIO
E2

Minimum and Maximum Values (Analog Channels)

All memory-mapped I/O units with analog capability automatically keep track of minimum and maximum values on analog channels.

You can read these values using the memory map (see "(Expanded) Analog Channel Read—Read Only" on page 88). You can also read and clear them at the same time (see "(Expanded) Analog Channel Read & Clear—Read/Write" on page 87).

PR1
RIO
PAC-R
EB
SB
UIO
EIO
SIO
E2

Offset and Gain (Analog Channels)

Memory-mapped I/O units with analog capability can calculate offset and gain for analog input channels. Calculate offset first, and then calculate gain.

For SNAP, see the *PAC Manager User's Guide* for instructions.

NOTE: If you are using Modbus/TCP, you will need to calculate the offset and gain yourself. Then you can write offset and gain values to the I/O unit. See the PAC Manager User's Guide for more information.

PR1
RIO
PAC-R
EB
SB
UIO
EIO
SIO
E2

Clamping (Analog Channels)

SNAP Ethernet-based I/O units with analog capability can clamp values sent to analog output channels so they do not go above or below a specific limit.

For example, if you are using a 0–10 VDC output module, but the device attached to one of its channels can only handle a maximum of 5 VDC, you can set an upper clamp of 5 VDC for that channel.

The values for upper and lower clamp are set in engineering units. Set upper and lower clamps when configuring the channel.

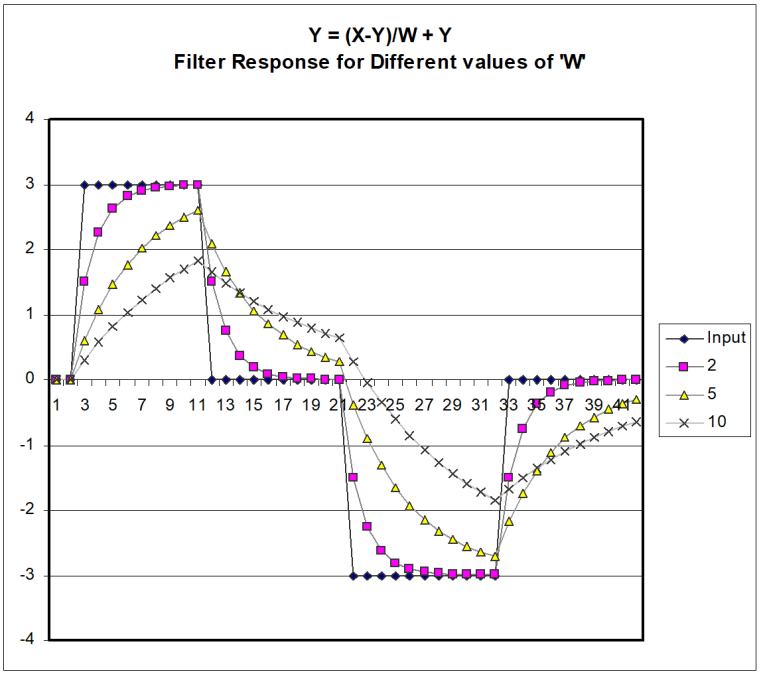
PR1
RIO
PAC-R
EB
SB
UIO
EIO
SIO

Average Filter Weight (Analog Channels)

SNAP Ethernet-based I/O units can use a filter weight to smooth analog input signals that are erratic or change suddenly.

The formula used for filtering is Y = (X - Y)/W + Y, where Y is the filtered value, X is the new unfiltered value, and W is the filter weight.

The following graph shows the effect of filter weights (W) 2, 5, and 10 on a step input signal:



As this graph shows, the larger the filter weight (W) you use, the smoother the analog signal.

A filter weight of zero turns off the calculation. Values less than or equal to 0.5 are changed to zero, since those values would cause an unstable signal.

Filtering is applied to values that are in engineering units, including minimum and maximum values. Filtering does not apply to values that are in counts. Set filter weight when configuring the analog channel.

Scratch Pad

PR1
PAC-R
PAC-S
EB
SB
UIO
EIO
LCE

groov I/O units, *groov* RIO modules, SNAP PAC S-series and SNAP-LCE standalone controllers, SNAP PAC R-series and SNAP Ultimate on-the-rack controllers, and SNAP PAC and SNAP Ethernet brains contain Scratch Pad areas within their memory maps. (SNAP Simple brains and E1 and E2 brain boards do not contain a Scratch Pad.) Scratch Pad areas can be used for two main purposes:

- As a place to hold data being transferred from one peer to another on the network (*groov* EPIC, *groov* RIO, SNAP PAC S-series and R-series, SNAP-LCE, and SNAP Ultimate only)
- As a virtual notebook for keeping track of events and alarms (SNAP PAC R-series, SNAP PAC brains, SNAP Ultimate, and SNAP Ethernet only)

The Scratch Pad is user-defined, meaning that you define and use its addresses to fit your needs, and you can redefine them whenever necessary. The Scratch Pad area includes up to four sections, depending on device type, to accommodate different types of data: bits, strings, floats, and integers.

- The Scratch Pad bits section is a 64-bit mask.
- The Scratch Pad strings section is a table of 64 elements. Each element can hold 128 characters or 128 bytes of binary data.
- The Scratch Pad float section is a table of 10,240 elements; each float is four bytes.
- The Scratch Pad 32-bit integer section is also a table of 10,240 four-byte elements.
- The Scratch Pad 64-bit integer section is a table of 1024 eight-byte elements.

NOTE: Scratch Pad float and 32-bit integer tables are not made up of contiguous addresses in the memory map; each table is in two address sections. You won't notice this if you are using PAC Control Scratch Pad commands, but if you

are addressing these tables in another application, check the memory map appendix in the OptoMMP Protocol Guide *to make sure you have the correct addresses for the table elements you want.*

Scratch Pad strings, floats, and integers are available for *groov* EPIC, *groov* RIO, SNAP PAC R-series, S-series, and SNAP Ultimate I/O and are primarily used to transfer data from one peer to another on the network. For more information on using the Scratch Pad in this way, see "I/O Units—Scratch Pad Commands" in Chapter 10 of the PAC Control User's Guide. (For SNAP, you can also use PAC Manager for one-time reads and writes.)

Scratch Pad bits are available for both standalone and on-the-rack controllers, groov RIO modules, and SNAP Ethernet I/O units. Controllers, *groov* RIO, and Ultimate I/O units usually use them in the same way as strings, floats, and integers—they're just another data format—but in Ethernet I/O units, Scratch Pad bits are primarily used for tracking events and alarms.

PR1
PAC-R
EB
SB
UIO
EIO

Using Scratch Pad Bits for Events and Alarms

When Scratch Pad bits are used to track events and alarms, the 64 bits in the mask do not represent channel numbers. Instead, they represent whatever you decide they should be. For example, you might decide that bit 1 in the Scratch Pad will indicate a temperature level in Vat #12 (if the temperature reaches 48 °C, bit 1 is turned on). Bit 2 might indicate the status of Pump A (if the pump is off, the bit is off; if the pump is on, the bit is on).

Because you can use Scratch Pad bits to keep track of events and alarms, you can set up reactions based on a variety of conditions. In the example above, you could set up a reaction on an EB brain that sends a stream packet if bit 1 is on and bit 2 is off.

Cascading Events, Alarms, and Reactions

Scratch Pad bits are really a way to set up cascading events and reactions (that is, a series of events and reactions dependent on each other). For example, the first event in the cascade could be the temperature in Vat #12 reaching 40 degrees, and the reaction to it is setting Scratch Pad bit 1. The second event in the cascade is that Scratch Pad bit #1 is set, and the reaction to that is some other action. A cascade of any number of events and reactions can be configured, as needed.

Using Event/Reactions

PAC-R
EB
SB
UIO
EIO

(Does not apply to *groov* I/O units or *groov* RIO modules.) Event/reactions are available on SNAP PAC R-series, SNAP PAC EB and SB brains, SNAP Ultimate, and SNAP Ethernet I/O units. SNAP Simple I/O units and E1 and E2 brain boards do not have event/reaction capability.

CAUTION: *Event/reactions occur on the I/O side of a SNAP PAC R-series or SNAP Ultimate controller, independently of any PAC Control strategy running on the control side. If you are using PAC Control, it is best to use flowchart logic to handle reactions to events. If you do set up event/reactions, be very careful that they do not conflict with PAC Control logic.*

PAC-R
EB
SB
UIO
EIO

Types of Events, Alarms, and Reactions

NOTE: groov I/O units and SB brains do not support serial events and reactions nor reactions requiring an Ethernet network, such as sending email.

Effect of Firmware on Events and Reactions

The following table shows the types of events and reactions available, depending on your processor and the SNAP PAC firmware version you are using. The event or reaction can consist of one or a combination of the following. The reaction can take place immediately or after a delay.

	PAC Firmware ≥ 8.1		PAC Firmware ≤ 8.0	
	PAC-R, EB	SB	PAC-R, EB	UIO, EIO
Events				
On/off state of digital channel on 4-channel module	●	●	●	●
State of on-latch or off-latch for digital channel on 4-ch mod	●	●		
On/off state of digital channel on HDD module	●	●		
State of on-latch or off-latch for digital channel on HDD mod	●	●		
High or low value of analog channel (in EU)	●	●	●	●
Number on a digital counter or high or low number on quadrature counter	●	●	●	●
Analog channel value or quadrature counter that is outside allowable range	●	●	●	●
State of a bit in the Scratch Pad bits area	●	●	●	●
State of a bit in the Scratch Pad integer 64 area	●	●		
Specific string received by serial module	●		●	●
Reactions				
Turn on/off digital channel on 4-channel module	●	●	●	●
Turn on/off digital channel on HDD module	●	●		
Clear on-latch or off-latch on 4-channel or HDD module	●	●		
Copy data from one memmap location to another	●	●	●	●
Log data	●	●	●	●
Turn on or off a bit in the Scratch Pad bits area	●	●	●	●
Turn on or off a bit in the Scratch Pad integer 64 area	●	●		
Send stream packet	●		●	●
Send email message	●		●	●
Send string through a serial module to a serial device	●		●	●
Send SNMP trap	●		●	●

The following table shows the number and type of events available, depending on the processor and the firmware version.

Event Type	PAC Firmware ≥ 8.1		PAC Firmware ≤ 8.0	
	PAC-R, EB	SB	PAC-R, EB	UIO, EIO
Digital events–Expanded (formerly called Timers)	512	512	64	64
Digital events–Old	128	128	128	128
Alarm events	64	64	64	64
Serial events	32	n/a	32	32

Note that the memory map section formerly called Timers, which provided digital events with a delay between an event and the reaction to it, has been expanded in firmware 8.1 to include additional options

such as latches and HDD modules. All new digital events should be configured in Digital Events - Expanded to take advantage of the new flexibility.

Digital events you already configured still exist in Digital Events - Old. Timers you already configured still exist in Digital Events - Expanded.

Steps for Configuring Events and Reactions—PAC Firmware R8.1 and Higher

The following table shows steps you would use to configure possible events and reactions if you are using firmware R8.1 or higher with SNAP PAC I/O units. (For older firmware, see "Steps for Configuring Events and Reactions—PAC Firmware R8.0 and Lower" on page 42.) Page numbers refer you to the memory map addresses in Appendix A: Opto 22 Hardware Memory Map that you would use for configuration.

See explanations starting on page 44 for important information you'll need to set up the different kinds of events and reactions.

Event	Reaction	Configuration Steps	See page
If digital channel is on/off ***or*** If on-latch or off-latch is set	Turn digital channel on/off on same I/O unit ***or*** clear on-latch or off-latch on same I/O unit	Configure Expanded Digital Events, with or without delay	127
	Turn digital channel on/off on different I/O unit ***or*** clear on-latch or off-latch on different I/O unit ***or*** log data ***or*** copy memory map data ***or*** send message (stream, email, serial, or SNMP trap).	1. Configure Expanded Digital Events—set Scratch Pad bit 2. (Email message only) Configure Email (Streaming only) Configure Streaming (SNMP only) Configure SNMP 3. (Except data logging) Configure Event Messages—send message or data (Data logging) Configure Data Logging and configure Email (optional)	127 143 119 114 141 154 143
If analog channel value (Engineering Units) goes above or below a specified value ***or*** If digital counter reaches a specified value	Turn digital channel on/off on same I/O unit ***or*** clear on-latch or off-latch on same I/O unit	1. Configure Alarm Events (high alarm or low alarm)—set Scratch Pad bit 2. Configure Expanded Digital Events—turn on/off channel or clear latch	140 127
	Turn digital channel on/off on different I/O unit ***or*** clear on-latch or off-latch on different I/O unit ***or*** log data ***or*** copy memory map data ***or*** send message (stream, email, serial, or SNMP trap).	1. Configure Alarm Events (high alarm or low alarm)—set Scratch Pad bit 2. (Delay only) Configure Expanded Digital Events—set time delay and set a Scratch Pad bit after the delay 3. (Email message only) Configure Email (Streaming only) Configure Streaming (SNMP only) Configure SNMP 4. (Except data logging) Configure Event Messages—send message or data based on timer-expired bit (Data logging) Configure Data Logging based on timer-expired bit and configure Email (optional)	140 127 143 119 114 141 154 143

Event	Reaction	Configuration Steps	See page
If analog channel value (Engineering Units) or quadrature counter goes outside an allowable range	Turn digital channel on/off on same I/O unit ***or*** clear on-latch or off-latch on same I/O unit	1. Configure Alarm Events (deviation alarm)—set Scratch Pad bit 2. Configure Expanded Digital Events—turn on/off channel	140 127
	Turn digital channel on/off on different I/O unit ***or*** clear on-latch or off-latch on different I/O unit ***or*** log data ***or*** copy memory map data ***or*** send message (stream, email, serial, or SNMP trap).	1. Configure Alarm Events (deviation alarm)—set Scratch Pad bit 2. (Delay only) Configure Expanded Digital Events—set time delay and set a Scratch Pad bit after the delay 3. (Email message only) Configure Email (Streaming only) Configure Streaming (SNMP only) Configure SNMP 4. (Except data logging) Configure Event Messages—send message or data based on timer-expired bit (Data logging) Configure Data Logging based on timer-expired bit and configure Email (optional)	140 127 143 119 114 141 154 143
If a specific string is received by a serial module	Turn digital channel on/off on same I/O unit ***or*** clear on-latch or off-latch on same I/O unit	1. Configure Serial Events—set Scratch Pad bit 2. Configure Expanded Digital Events—turn on/off channel or clear latch	144 127
	Send SNMP trap	1. Configure Serial Events—set Scratch Pad bit 2. (Delay only) Configure Expanded Digital Events—set time delay and set a Scratch Pad bit after the delay 3. Configure SNMP 4. Configure Event Messages—send trap based on timer-expired bit	144 127 114 141
	Send one-time email	1. Configure Serial Events—send email 2. Configure Email	144 143
	Turn digital channel on/off on different I/O unit ***or*** clear on-latch or off-latch on different I/O unit ***or*** log data ***or*** copy memory map data ***or*** send message (stream, email, serial, or SNMP trap).	1. Configure Serial Events—set Scratch Pad bit 2. (Except data logging) Configure Event Messages—send message or data (Data logging) Configure Data Logging and configure Email (optional)	144 141 154 143
		1. Configure Serial Events—set Scratch Pad bit 2. (Delay only) Configure Expanded Digital Events—set time delay and set a Scratch Pad bit after the delay 3. (Email message only) Configure Email (Streaming only) Configure Streaming 4. (Except data logging) Configure Event Messages—send message or data based on timer-expired bit (Data logging) Configure Data Logging based on timer-expired bit and configure Email (optional)	144 127 143 119 141 154 143

Steps for Configuring Events and Reactions—PAC Firmware R8.0 and Lower

(Does not apply to *groov* I/O units.) The following table shows steps you would use to configure possible events and reactions if you are using SNAP firmware R8.0 or lower with PAC Manager 8.0 or 8.1 (see "Types of Events, Alarms, and Reactions" on page 39 for more details). Page numbers refer you to the memory map addresses in Appendix A that you would use for configuration.

See explanations starting on page 44 for important information you'll need to set up the different kinds of events and reactions.

Event	Reaction	When?	Configuration Steps	See page
If 4-channel digital channel is on/off	Turn 4-channel digital channel on/off (on same I/O unit)	Now	Configure Digital Events	127
		After a delay	Configure Timers	127
	Turn 4-channel digital channel on/off (on different I/O unit) ***or*** Log data ***or*** Copy memory map data ***or*** Send message (stream, email, serial, or SNMP trap).	Now	1. Configure Digital Events—set Scratch Pad bit 2. (Except data logging) Configure Event Messages—send message or data (Data logging) Configure Data Logging and configure Email (optional)	127 141 154 143
		After a delay	1. Configure Timers—set Scratch Pad bit 2. (Email message only) Configure Email (Streaming only) Configure Streaming (SNMP only) Configure SNMP 3. (Except data logging) Configure Event Messages—send message or data (Data logging) Configure Data Logging and configure Email (optional)	127 143 119 114 141 154 143
If analog channel value (Engineering Units) goes above or below a specified value OR If digital counter reaches a specified value	Turn 4-channel digital channel on/off (on same I/O unit).	Now	1. Configure Alarm Events (high alarm or low alarm)—set Scratch Pad bit 2. Configure Digital Events—turn on/off channel	140 127
		After a delay	1. Configure Alarm Events (high alarm or low alarm)—set Scratch Pad bit 2. Configure Timers—turn on/off channel	140 127
	Turn 4-channel digital channel on/off (on different I/O unit) ***or*** Copy memory map data ***or*** Log data ***or*** Send message (stream, email, serial, or SNMP trap).	Now	1. Configure Alarm Events (high alarm or low alarm)—set Scratch Pad bit 2. (Except data logging) Configure Event Messages—send message or data (Data logging) Configure Data Logging and configure Email (optional)	140 141 154 143
		After a delay	1. Configure Alarm Events (high alarm or low alarm)—set Scratch Pad bit 2. Configure Timers—set time delay and set a Scratch Pad bit after timer expires 3. (Email message only) Configure Email (Streaming only) Configure Streaming (SNMP only) Configure SNMP 4. (Except data logging) Configure Event Messages—send message or data based on timer-expired bit (Data logging) Configure Data Logging based on timer-expired bit and configure Email (optional)	140 127 143 119 114 141 154 143

Event	Reaction	When?	Configuration Steps	See page
If analog channel value (Engineering Units) or quadrature counter goes outside an allowable range	Turn 4-channel digital channel on/off (on same I/O unit)	Now	1. Configure Alarm Events (deviation alarm)—set Scratch Pad bit 2. Configure Digital Events—turn on/off channel	140 127
		After a delay	1. Configure Alarm Events (deviation alarm)—set Scratch Pad bit 2. Configure Timers—turn on/off channel	140 127
	Turn 4-channel digital channel on/off (on different I/O unit) ***or*** Copy memory map data ***or*** Log data ***or*** Send message (stream, email, serial, or SNMP trap).	Now	1. Configure Alarm Events (deviation alarm)—set Scratch Pad bit 2. (Except data logging) Configure Event Messages—send message or data (Data logging) Configure Data Logging and configure Email (optional)	140 141 154 143
		After a delay	1. Configure Alarm Events (deviation alarm)—set Scratch Pad bit 2. Configure Timers—set time delay and set a Scratch Pad bit after timer expires 3. (Email message only) Configure Email (Streaming only) Configure Streaming (SNMP only) Configure SNMP 4. (Except data logging) Configure Event Messages—send message or data based on timer-expired bit (Data logging) Configure Data Logging based on timer-expired bit and configure Email (optional)	140 127 143 119 114 141 154 143
If a specific string is received by a serial module	Turn4-channel digital channel on/off (on same I/O unit)	Now	1. Configure Serial Events—set Scratch Pad bit 2. Configure Digital Events—turn on/off channel	144 127
		After a delay	1. Configure Serial Events—set Scratch Pad bit 2. Configure Timers—turn on/off channel	144 127
	Send SNMP trap	Now	1. Configure Serial Events—send SNMP trap 2. Configure SNMP	144 114
		After a delay	1. Configure Serial Events—set Scratch Pad bit 2. Configure Timers—set time delay and set a Scratch Pad bit after timer expires 3. Configure SNMP 4. Configure Event Messages—send trap based on timer-expired bit	144 127 114 141
	Send one-time email	Now	1. Configure Serial Events—send email 2. Configure Email	144 143
	Turn 4-channel digital channel on/off (on different I/O unit) ***or*** Copy memory map data ***or*** Log data ***or*** Send message (stream, serial, or multiple e-mails)	Now	1. Configure Serial Events—set Scratch Pad bit 2. (Except data logging) Configure Event Messages—send message or data (Data logging) Configure Data Logging and configure Email (optional)	144 141 154 143
		After a delay	1. Configure Serial Events—set Scratch Pad bit 2. Configure Timers—set time delay and set a Scratch Pad bit after timer expires 3. (Email message only) Configure Email (Streaming only) Configure Streaming 4. (Except data logging) Configure Event Messages—send message or data based on timer-expired bit (Data logging) Configure Data Logging based on timer-expired bit and configure Email (optional)	144 127 143 119 141 154 143

PAC-R
EB
SB
UIO
EIO

Using Digital Events and Reactions

NOTE: Availability varies depending on I/O processor, firmware, and module. See "Types of Events, Alarms, and Reactions" on page 39.

(Does not apply to *groov* I/O units or *groov* RIO modules.) In a digital event, the I/O unit monitors one or more inputs, outputs, and Scratch Pad bits for a match to a specific pattern (the event). When the pattern is

matched, the I/O unit reacts in a predetermined way. The reaction can turn digital channels on or off and can also set bits in the Scratch Pad. You can configure up to 128 digital events and reactions.

Digital event/reactions can be as simple as turning on a light (reaction) when a door opens (event). They can also be very complex, depending on your needs. For example, suppose you need to monitor a critical group of switches. If switches 1, 2, and 3 are all off at the same time, you want to turn on an emergency light and sound an alarm. You can set up a digital event for the state of the three switches, and a reaction that automatically turns on the emergency light and alarm.

In addition to digital states, events can include alarm or other conditions noted in the Scratch Pad. For instance, to regulate the temperature of a room, you might set up an alarm event that turns on a bit in the Scratch Pad when the temperature reaches 78° F (see "Using Alarms and Reactions" on page 48). Then you would set up a digital event/reaction to turn on a fan when that Scratch Pad bit is on.

NOTE: If you want to turn on or off digital channels that are located on a different I/O unit, you can do so by using the memory map copying feature when setting up event messages (see page 50).

Digital On/Off and Scratch Pad Masks

Both events and reactions are in the form of a mask. Digital channel masks represent 64 possible digital states; you choose whether these represent channel states or on-latch or off-latch states. Scratch Pad masks represent whatever you decide each bit should be.

For each digital event/reaction, you set up two to eight masks (up to four for the event and up to four for the reaction), as shown below.

For the event: The table below shows possible triggers for the event, in the form of four masks. You can configure only Trigger #1, only Trigger #2, or both. If you configure both, both must be true for the event to be true. Choose the trigger(s) you want to use; then set up the masks.

Trigger #1		Trigger #2	
On mask	**Off mask**	**On mask**	**Off mask**
Digital channel state Digital channel on-latch Digital channel off-latch HDD channel state HDD on-latches HDD off-latches Scratch Pad bits	Digital channel state Digital channel on-latch Digital channel off-latch HDD channel state HDD on-latches HDD off-latches Scratch Pad bits	Scratch Pad bits Scratch Pad Integer 64 Digital channel state Digital channel on-latch Digital channel off-latch	Scratch Pad bits Scratch Pad Integer 64 Digital channel state Digital channel on-latch Digital channel off-latch

For the reaction: This table shows possible reactions, again in the form of four masks. You can configure only Reaction #1, only Reaction #2, or both. When the event occurs, all configured reactions will take place. Choose the reaction(s) you want to occur, and then set up the masks.

Reaction #1		Reaction #2	
On mask	**Off mask**	**On mask**	**Off mask**
Set digital channel state Clear digital channel latch Set HDD channel state Clear HDD latch Set Scratch Pad bits	Set digital channel state Clear digital channel latch Set HDD channel state Clear HDD latch Set Scratch Pad bits	Set Scratch Pad bits Set Scratch Pad Integer 64 Set digital channel state Clear digital channel latch	Set Scratch Pad bits Set Scratch Pad Integer 64 Set digital channel state Clear digital channel latch

NOTE: Trigger #1 does NOT control Reaction #1; Trigger #2 does not control Reaction #2. Instead, all the masks work as a group. All the event masks must be a match for the I/O unit to set the reaction(s), and if the event occurs, any and all reactions will be set. If it doesn't matter whether a specific channel or bit is on or off, leave its value at zero in both the on mask and the off mask.

To choose the triggers and reactions from the tables above, you also set up another mask: the event detail mask (see "Event Detail Mask," below, for examples).

When you configure events and reactions, the masks are in hex notation. If you are setting up a Digital On mask for channels on the first two modules, for example, you might do so as follows:

Module position:	1				0			
Channel number:	3	2	1	0	3	2	1	0
State:	On	–	On	On	–	–	–	On
Binary notation:	1	0	1	1	0	0	0	1
Hex notation:	B				1			

(For more information on mask data format, see page 58.)

You can also configure the I/O unit to send a message as a reaction to digital events. See page 50.

Event Detail Mask

In addition to the two to eight on/off bitmasks mentioned above, there's also a separate bitmask that indicates the details for the event—which triggers to use and which reactions should occur. For Event 0, for example, this mask goes in memory map address FFFF F0D4 0044.

The table on the following page shows which bits to set in this detail mask to achieve the triggers and reactions you want. In the table the triggers and reactions are separated for clarity, but you build only one mask that includes all the elements you need. See the example below the table.

Remember that bit numbering starts at 0.

Event Detail Mask Bits

	For this	Set these bits	Binary example	Hex example
Event	Trigger #1			
	Digital Channel State	None	0000 0000 0000 0000 0000 0000 0000 0000	0x00000000
	Digital Channel On-Latch	1, 2	0000 0000 0000 0000 0000 0000 0000 0110	0x00000006
	Digital Channel Off-Latch	1	0000 0000 0000 0000 0000 0000 0000 0010	0x00000002
	HDD Channel State	4	0000 0000 0000 0000 0000 0000 0001 0000	0x00000010
	HDD Channel On-Latch	1, 2, 4	0000 0000 0000 0000 0000 0000 0001 0110	0x00000016
	HDD Channel Off-Latch	1, 4	0000 0000 0000 0000 0000 0000 0001 0010	0x00000012
	Scratch Pad Bits	15	0000 0000 0000 0000 1000 0000 0000 0000	0x00008000
	Trigger #2			
	Scratch Pad Bits	None	0000 0000 0000 0000 0000 0000 0000 0000	0x00000000
	Scratch Pad Integer 64	6	0000 0000 0000 0000 0000 0000 0100 0000	0x00000040
	Digital Channel State	16	0000 0000 0000 0001 0000 0000 0000 0000	0x00010000
	Digital Channel On-Latch	16, 17, 18	0000 0000 0000 0111 0000 0000 0000 0000	0x00070000
	Digital Channel Off-Latch	16, 17	0000 0000 0000 0011 0000 0000 0000 0000	0x00030000

	For this	Set these bits	Binary example	Hex example
Reaction	Reaction #1			
	Digital Channel State	None	0000 0000 0000 0000 0000 0000 0000 0000	0x00000000
	Clear Digital Channel Latches	3	0000 0000 0000 0000 0000 0000 0000 1000	0x00000008
	HDD Channel State	5	0000 0000 0000 0000 0000 0000 0010 0000	0x00000020
	Clear HDD Latches	3, 5	0000 0000 0000 0000 0000 0000 0010 1000	0x00000028
	Scratch Pad Bits	20	0000 0000 0001 0000 0000 0000 0000 0000	0x00100000
	Reaction #2			
	Scratch Pad Bits	None	0000 0000 0000 0000 0000 0000 0000 0000	0x00000000
	Scratch Pad Integer 64	7	0000 0000 0000 0000 0000 0000 1000 0000	0x00000080
	Digital Channel State	19	0000 0000 0000 1000 0000 0000 0000 0000	0x00080000
	Clear Digital Channel Latches	21	0000 0000 0010 0000 0000 0000 0000 0000	0x00200000
	How reaction occurs (applies to both Reaction #1 and Reaction #2)			
	Reaction occurs once*	8	0000 0000 0000 0000 0000 0001 0000 0000	0x00000100
	* By default, the reaction occurs continuously. See "How Digital Events Trigger Reactions" on page 47).			

Event Detail Mask Example

In the table above, the triggers and reactions are separated for clarity, but in practice you build only one mask that includes all the elements you need.

For example, suppose you want to use two triggers and one reaction for Event 0, like this:

Trigger #1 = Digital channel on-latch
Trigger #2 = Scratch Pad bit
Reaction #1 = [not used]
Reaction #2 = Scratch Pad Integer 64
And you want the reaction to occur only once, not continuously.

Looking at the table, you see you must set the following bits (don't forget, bit numbering starts at 0):

Trigger #1 = Digital channel on-latch = bits 1 and 2
Trigger #2 = Scratch Pad bit = [none]
Reaction #1 = [not used] = [none]
Reaction #2 = Scratch Pad Integer 64 = bit 7
Reaction occurs once = bit 8

So in memory map address FFFF F0D4 0044, you enter a hex mask you build like this:

Bit #:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0
Hex:	0				0				0				0				0				1				8				6			

How Digital Events Trigger Reactions

Reactions to digital events are level-triggered, not edge-triggered, by default. The I/O unit continually checks the digital state to see if it matches the event. The I/O unit sends the reaction as soon as the state matches the event, and the I/O unit continues to send the reaction until the state changes. On a SNAP PAC I/O unit with 8.1 firmware or higher, however, you can set the event to trigger the reaction just once, rather than continuously.

In either case, if the state changes so that it no longer matches the event, the I/O unit does NOT reverse the reaction.

Digital Event/Reaction Example

For example, suppose you have set up an event/reaction to turn on a light when a door is open. As soon as the event occurs (the door opens), the I/O unit sends the reaction (turn on the light). Unless you have set the reaction to be triggered just once, the reaction continues to be sent as long as the door is open.

When the door is shut, the I/O unit does NOT turn the light off. To turn off the light when the door is shut, you need to set up a second event/reaction.

Suppose the input for the door's status is on channel 0, and the output for the light is on channel 5. Here are the two event/reactions to turn on the light when the door is open, and turn off the light when the door is shut:

Event #0:	IF	Mod 0 Pt 0 (Door) is	OFF (Open)
Reaction #0:	THEN	Turn Mod 1 Pt 1 (Light)	ON
Event #1:	IF	Mod 0 Pt 0 (Door) is	ON (Closed)
Reaction #1:	THEN	Turn Mod 1 Pt 1 (Light)	OFF

PAC-R
EB
SB
UIO
EIO

Using Alarms and Reactions

(Does not apply to *groov* I/O units or *groov* RIO modules.) A reaction can also be set up as a response to an alarm. You can configure alarms for analog channels or digital counters. (See "Alarm Event Settings—Read/Write" on page 140). For example, you could trigger an alarm when the pressure in a tank rises above a certain level, or when a specific number of boxes on a conveyor have passed through a beam sensor. For each alarm, you configure a suitable reaction.

For analog channels, alarms are based on the analog input value. For digital channels, alarms are based on the counter value. For each channel, you can configure any or all of the following alarms:

- Deviation alarm—sets a range on either side of the current value that is acceptable; beyond that range, the reaction occurs. For example, suppose you are monitoring temperature. If the current value is 80 and you set a deviation limit of 6, the reaction will not occur unless the value drops below 74 or rises above 86.

  NOTE: When a reaction occurs, the deviation limit stays the same, but the value that set off the reaction becomes the new deviation value. In this example, if the temperature drops to 73, the reaction occurs. Six is still the deviation limit, but now 73 is the deviation value; another reaction will not occur unless the value drops below 67 or rises above 79.

  Also, as soon as the new deviation value is set, the alarm Scratch Pad bit is turned back off (because it is no longer in an alarm state); this change happens almost immediately. If you need to know that a deviation alarm occurred, you can set up another reaction to capture the occurrence. That reaction might start a timer or send an email that requires acknowledgment, for example.

- High-limit alarm—sets a fixed upper limit. If the analog value or counter is higher than the high limit, the reaction occurs.
- Low-limit alarm—sets a fixed lower limit. If the analog value or counter is lower than the low limit, the reaction occurs.

How Alarms Trigger Reactions

Reactions to alarms are edge-triggered, not level-triggered, and when the alarm state changes, the reaction is automatically reversed. The I/O unit sends the reaction just once, as soon as the alarm occurs (at the "edge" of the alarm). The I/O unit does not send the reaction again until the alarm occurs again. If the alarm stops, however, the I/O unit *reverses* the reaction. (See the note above on Deviation alarms.)

For example, suppose you set up a high-limit alarm that turns on a Scratch Pad bit that will turn on a fan if the temperature goes over 70°. As soon as the alarm state occurs (the temperature goes over 70°), the I/O unit sends the reaction (turns on the bit to turn on the fan). If the temperature remains above 70°, the I/O unit does not continue to turn on the fan bit; the bit just stays on.

When the temperature falls back below the high limit (70° minus whatever deadband you have set), the I/O unit automatically reverses the reaction by turning the Scratch Pad bit off. (To turn the fan off, you would have to set up a reaction for the off bit, turning the fan off.)

Notice that the reaction and its reversal are absolute; they do not depend on the pre-alarm condition. For example, if the bit to turn on the fan was already on at the time the temperature rose above 70°, the reaction would turn the bit on even though it was already on. When the temperature fell back below 70°, the I/O unit would *not* return the fan bit to its pre-alarm condition (on); it would turn the bit off.

PAC-R EB UIO EIO

Using Serial Events and Reactions

(Does not apply to *groov* I/O units, *groov* RIO modules, or SB brains.) If you are using Opto 22 serial communication modules with a SNAP PAC R-series, SNAP PAC EB, SNAP Ultimate, or SNAP Ethernet I/O unit, you can configure a serial event to send a serial message, to send an SNMP trap, or to turn bits in the Scratch Pad on or off when a specific string is received from one or more modules. See "Serial Event Configuration—Read/Write" on page 144 or "Wiegand Serial Event Configuration—Read/Write" on page 145.

Before you configure serial events and reactions, make sure you have configured the serial modules. (See page 107 or page 108.)

PAC-R EB UIO EIO

Using SNMP in Reactions

(Does not apply to *groov* I/O units or *groov* RIO modules.) To send an SNMP trap as a reaction to an event, you must also tell the I/O unit information about the SNMP agent and access privileges for hosts on the network.

SNMP Access Privileges

Community groups control access to information from the SNAP Ethernet-based I/O unit. The first community group, public, is set up for you. All hosts on the network are part of the public group; all can read and write I/O unit data but cannot receive traps. You can change or delete this public group if necessary.

In order to receive traps, a host must be a registered *management host* and be part of a community group that does have access privileges for traps. Once a registered management host becomes part of a community group, that group is no longer available to non-registered hosts. It includes only the hosts registered to it.

You must set up the additional community groups you need, either in PAC Manager or in your custom application. See "SNMP Configuration—Read/Write" on page 114. Note that SNMP configuration must be stored to flash memory and the I/O unit restarted for it to take effect.

SNMP Traps

The SNAP Ethernet-based I/O unit can send three kinds of traps:

- Authentication trap—sent when a host requests data that is outside its access permissions
- Cold start trap—sent whenever the I/O unit is turned on
- Exception trap—sent in reaction to an event; an exception trap is a type of event message.

Authentication and cold start traps require no configuration and can simply be enabled. Exception traps must be configured when you set up event messages.

PAC-R EB UIO EIO

Setting Up Event Messages

(Does not apply to *groov* I/O units or *groov* RIO modules.) You may need to send a message—via email, data streaming, SNMP, or a serial module—from the SNAP Ethernet-based I/O unit when a specific event occurs. For example, you could send a message if a digital channel is on, if an analog channel reaches a certain value, or if a specific string is received through a serial module. You can send one type of message or more. Your custom application monitors the event and triggers the message you have configured.

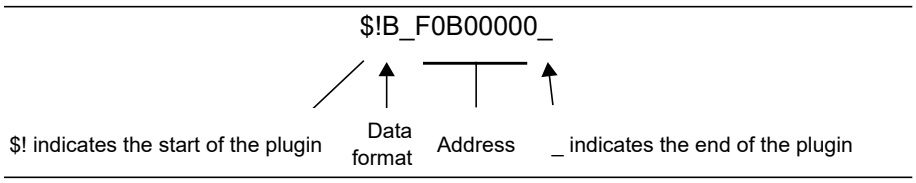
You can configure up to 128 messages, either in PAC Manager or in your custom application. See "Event Message Configuration—Read/Write" on page 141 for memory map addresses to use.

Copying Binary or Memory Map Data

You can use memory map copying to do the following:

- Copy data on the same I/O unit.
- Copy data to a memory map location on another unit.

Set up memory map copying when you configure event messages. For Message Text, enter a plugin containing a memory map address to write *from* (the source address), in the following format:



or a four-byte constant, in this format:

```
&#x00000001_
```

NOTE: Constants must be written in exactly four bytes (8 hex characters).

While the data format indicator in the plugin can be other types (D=integer, F=float), B is typically used for memory map copying. The other types copy a *string representation* of the data, because plugins are primarily used for generating messages and emails. For more about plugins, see "Using Plugins" on page 50.

PAC-R EB UIO EIO

Using Email

(Does not apply to *groov* I/O units or *groov* RIO modules.) You can send an email message in response to an event. In addition to setting up the email message when you configure event messages, you also need to tell the I/O unit where to send the email. See "Email Configuration—Read/Write" on page 143.

PAC-R EB UIO EIO

Using Plugins

(Does not apply to *groov* I/O units or *groov* RIO modules.) Several plugins are available for use in event/reactions and messages.

To do this	Use this plugin	In these places
Include the pattern string from a serial communication module.	`$!_str_`	Serial event/reactions
Show which serial port sent the pattern string.	`$!_port_`	Serial event/reactions

To do this	Use this plugin	In these places
Include data from a memory map address. X = type of data (S=string representation of the data, D=integer, F=float, P=IP address, B=4 binary bytes) YYYYYYYY = memory map address (see examples below)	`$!X_YYYYYYYY_`	Serial event/reactions Event messages Memory map copying Email
Number emails with a sequence ID.	`$!_seqid_`	Email
Turn digital channels on or off using a bit mask.	`&#x00000000_`	Memory map copying Event messages

NOTE: For email messages, message text including plugins must be 126 bytes (characters) or less. The message length after all plugins have been expanded into their data values must be 255 bytes or less.

Examples: Including Data from Memory Map Addresses

Memory map addresses are shown in PAC Manager, or see Appendix A: Opto 22 Hardware Memory Map for the complete memory map. Here are a couple of examples:

To include the on/off state of a switch on module 0 channel 3, you would put this in the message:

```
$!D_F08000C0_
```

To include the temperature of an ICTD input on module 4 channel 0, you would use:

```
$!F_F0A00400_
```

Sending Binary Data in Event Messages

To send binary data in the text of an event message, begin with `&#x` and end with `_`. You can include any number of ASCII hex digits up to the 126-byte limit for the message field. You can also include multiple &#x plugins. This plugin is resolved after all other plugins have been resolved, and only just before sending the contents of the message field. Examples:

To include an embedded null (one binary character): `&#x00_`

To include a number of binary characters: `&#x0a0dCF0034_`

STREAMING DATA

PR1
RIO
PAC-R
EB
UIO
EIO
SIO

Most communication involves the two-step process of request and response. A faster way of getting information from an Ethernet-based I/O unit, however, is by streaming data[3]. Streaming does not use TCP/IP; it uses the User Datagram Protocol (UDP) instead.

NOTE: Because Modbus/TCP runs on TCP, not UDP, streaming data via Modbus/TCP is not possible. However, you can stream to a non-Modbus host at the same time you are using the Modbus/TCP protocol for another purpose.

Streaming is a fast way to get continuous information about I/O from the Ethernet-based I/O unit and is ideal for data acquisition applications. When it streams, the I/O unit sends data at regular intervals to specified IP addresses. You set up the interval, the IP addresses to receive the data, and (optionally) the port number. The I/O unit sends the data at the specified interval. The communication is one-way; the I/O unit does not wait for a response.

Note that *groov* EPIC processors and *groov* RIO modules have a built-in firewall. To allow streaming, you'll need to add a rule to allow outgoing communications on the port you want to use for streaming. For instructions to

[3] If you don't need to stream the data, you can use *Packed Data* areas to get a large amount of data all at once. These areas put large amounts of related data into one area of the memory map so it's faster and easier to read in one transaction. For details, see "(Expanded) Digital Packed Data—Read Only" on page 91, "(Expanded) Digital Packed Must on/OFF (MOMO)—Read/Write" on page 91, "Analog EU or Digital Counter (Feature) Packed Data—Read" on page 139, and "Digital Packed Data—Read/Write" on page 139.

modify firewall rules in *groov* Manage, see the *groov EPIC User's Guide* (form 2267) or the *groov RIO User's Guide* (form 2324).

CAUTION: *If you stream to multiple IP addresses, and one or more of the streaming targets is either offline or not running the application that receives the stream, delays may occur. If a target is offline, the I/O unit will stop streaming while it tries to resolve the IP address. If the application is not running on the PC that receives the stream, the PC will send the I/O unit an error message; if the stream occurs frequently, the additional error messages can slow down the network.*

You can use either of two methods to stream data:

- Traditional streaming (page 52) uses the predefined Streaming area of the memory map (see page 138). Addresses are different for *groov* EPIC and *groov* RIO than for SNAP. For SNAP, this area is limited to a maximum of 64 channels of I/O on a full rack, with all I/O modules having 4 channels or less. This functionality started with the SNAP-B3000-ENET brain (our earliest Ethernet-based brain, first released in 1998), and you can still use it with newer brains if you want. However, newer brains can support I/O modules with up to 32 channels each and a full rack of 512 channels; use custom streaming to utilize all channels.
- Custom streaming (page 53) lets you stream other addresses of the memory map, either one contiguous area or a combination of separate addresses. Use custom streaming for *groov* EPIC, *groov* RIO, and I/O modules with more than four channels, or use it to define exactly the data you want in a stream.

Traditional Streaming

Traditional streaming involves two steps: configuring parameters on the I/O unit for streaming, and receiving data in your application.

Configuring Traditional Streaming

To set up the I/O unit for streaming data, you can use PAC Manager (for SNAP) or you can write to the memory map area for Streaming Configuration (see page 119).

- Write how often in milliseconds you want to receive the streamed data. If you are configuring streaming to use only as a reaction to a digital event or an analog alarm condition, set the streaming interval to 0 (send once).
- The data that is streamed is normally the whole Streaming section of the memory map (see page 138). To stream only a portion of the Streaming section, write the starting address and size of the data to stream.

  Note that high-density digital module data is not included in the Streaming section of the memory map. See "Custom Streaming" on page 53 for ways to get this data.
- Write the UDP port number on the PCs or devices that will receive streamed data. Your application must refer to this port number.
- Write the IP addresses of the hosts that should receive the data (the target addresses).
- To turn streaming on, write anything but a zero to the Streaming On/Off address. To turn streaming off, write a zero.

Receiving Traditional Streamed Data

As soon as you've configured parameters for streaming, the I/O unit starts sending the data you requested. Your application does not need to respond; it only needs to process the data.

Traditional Stream Packet Format

The stream packet consists of an IEEE 1394 header and data. Addresses will be zero-filled in areas that don't apply. For example, addresses that show analog data will be filled with zeros for channels that are digital.

The following table shows the format for the stream packet based on receiving the entire Streaming section of the memory map (see page 138). (If you are streaming data from other sections of the memory map, see "Custom Stream Packet Format" on page 54.)

Area	Number of Bytes	Description
Packet header	2	Total length of packet
	2	First byte is zero-filled; second byte contains transaction code 0x0A for an isochronous data block (4 bits) and synchronization code for Opto 22 use (4 bits).
Useful data	256	Analog values in Engineering Units (IEEE floats). Contains 4 bytes of data for each of 64 channels on 16 modules, starting with channel 0 on module 0. If the analog module contains more than 4 channels, only the first 4 channels are included.
	256	Channel feature data (counter data) (unsigned 32-bit integers).
	8	On/off state of all digital channels on 4-channel modules (mask). (Streaming does not provide data for high-density digital modules.)
	8	On-latch state (mask)
	8	Off-latch state (mask)
	8	Active counters (mask)
Unused data	56	Reserved for future data; zero-filled

For example, the first bytes of a stream packet might look like this:

These packet bytes:	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	→
Contain this hex data:	header				41	77	33	33	41	3F	AC	66	→
For these channels:	–				0				1				→
On module at position:	–				0								→

In the body of the stream packet, IEEE floats are arranged in low channel/low address order. See page 61 for an example. All masks in the stream packet are in Big Endian format, however, with higher-numbered channels in the lower-addressed byte. See page 58 for more information about how data in a mask is formatted.

Custom Streaming

Custom streaming lets you stream data from other memory map areas besides the traditional Streaming area. You can choose a single contiguous area starting with a specific memory map address, or you can choose several separated addresses and lump them together to access them all in one stream.

Configuring Custom Streaming

Use *groov* Manage (for *groov* I/O units and *groov* RIO modules), PAC Manager (for SNAP I/O units), or your custom application to write to the memory map areas.

1. For separated addresses, write to the Custom Configuration area of the memory map (page 133).
   The free .NET Framework OptoMMP SDK contains an example called "Custom Data Stream Demo" that can help you with this step.
2. For both contiguous and separated addresses, write to the memory map area for Streaming Configuration (see page 119).
   a. Write how often in milliseconds you want to receive the streamed data. If you are configuring streaming to use only as a reaction to a digital event or an analog alarm condition, set the streaming interval to 0 (send once).
   b. Write the starting address and size of the data to stream. For separated addresses, enter a starting address of F0D60000, the first address of the Custom Data Access area.

c. Write the UDP port number on the PCs or devices that will receive streamed data. Your application must refer to this port number.

d. Write the IP addresses of the hosts that should receive the data (the target addresses).

e. To turn streaming on, write anything but a zero to the Streaming On/Off address. To turn streaming off, write a zero.

Receiving Custom Streamed Data

As soon as you've configured parameters for streaming, the I/O unit starts sending the data you requested. Your application does not need to respond; it only needs to process the data.

Custom Stream Packet Format

The stream packet consists of an IEEE 1394 header and data. Addresses will be zero-filled in areas that don't apply. For example, addresses that show analog data will be filled with zeros for channels that are digital.

The following table shows the format for the streaming packet if you are receiving streamed data from any memory map addresses other than the Streaming area. (See "Traditional Stream Packet Format" on page 52 for the Streaming area.)

Area	Number of Bytes	Description
Packet length	2	Number of bytes in this packet
Zero byte	1	Always zero
Transaction byte	1	Upper nibble: A Lower nibble increases with each transmission.
Source MemMap address	4	Address(es) you configured in the Streaming configuration area or in the Custom Configuration area.
Data	Number of bytes you requested	Data format and organization of the memory map areas you requested. See Appendix for details.

In the body of the stream packet, IEEE floats are arranged in low channel/low address order. See page 61 for an example. All masks in the stream packet are in Big Endian format, however, with higher-numbered channels in the lower-addressed byte. See page 58 for more information about how data in a mask is formatted.

LOGGING DATA

PAC-R
EB
SB
UIO
EIO

(Does not apply to *groov* I/O units or *groov* RIO modules.) Your SNAP PAC R-series, SNAP PAC EB or SB, SNAP Ultimate, or SNAP Ethernet I/O unit includes a feature that allows data from memory map addresses to be recorded in a log file. The data from up to 64 memory map addresses can be logged, and all logged data is recorded in one file. The log file holds up to 300 lines of data; when it is filled, new entries replace the oldest ones.

Logging data requires two steps:

- Configure the events (Scratch Pad masks) that trigger logging and the memory map addresses to log data from.
- Read the data from the data log.

Configuring the Event and Memory Map Addresses to Log

Use either PAC Manager or your own application to configure the events that trigger logging (the Scratch Pad masks) and to tell the I/O unit which memory map addresses to log data from. "Data Logging Configuration—Read/Write" on page 154 shows the memory map addresses used to configure this information. Remember that the Scratch Pad masks work together: both masks must be a match to trigger logging. If it doesn't matter whether a specific bit is on or off, leave its value at zero in both the on mask and the off mask.

Reading the Data from the Data Log

The composite log file can be viewed through PAC Manager or emailed. (If the log will be emailed, remember to configure email.) The log file can also be accessed by a software application you develop. "Data Log—Read/Write" on page 155 shows the memory map addresses in which the data log is stored.

Each address in the log file consists of the date and time stamp, the memory map address the data is coming from, the format of the data, and the data itself. For example, address FFFFF3020000, the first data log address, might contain the following information:

Information in log file address (in hex):	07D0	06	1E	0E	23	2A	07	F0A0008C	00000066	41773333
Meaning:	2001	06	30	14	35	42	07	channel 2 analog max value	float	15.45
Description:	year	month	day	hour	minute	second	100th of a sec.	memory map address the data comes from	data format*	data
Number of bytes:	2	1	1	1	1	1	1	4	4	4

* Data format indicators (in hex) may be any of the following:

- 66 (f) for float
- 64 (d) for signed value
- 78 (x) for unsigned value.

In this example, the data is date/time stamped for 42.07 seconds after 2:35 P.M. on June 30, 2001. The data shows that the analog maximum value for channel 2 is 15.45 in Engineering Units (a float).

USING PID LOOPS

PAC-R
RIO
EB
UIO
EIO

What is a PID?

A proportional integral derivative (PID) control system (often referred to as a PID loop) monitors an input or process variable, compares the variable's current value to a desired value (a setpoint), and calculates an output to correct error between the setpoint and the variable. Because the calculation is complex, it is done by a mathematical formula that is adjusted (tuned) for each PID loop. The mathematical formulas vary, but all PID systems share these fundamental concepts:

- They evaluate an input or process variable against its setpoint.
- They control an output to correct the variable.
- The controller output consists of proportional, integral, and derivative calculations.
- The effect of proportional, integral, and derivative calculations is modified by user-determined P, I, and D constants.
- The P, I, and D constants need to be tuned for each system.

PID Loops on Ethernet-based I/O Units

PID loop control is provided on the following I/O units:

I/O Processor	Number of PID loops
GRV-EPIC-PR1	96
GRV-R7-MM1001-10	4

I/O Processor	Number of PID loops
SNAP-PAC-R1 SNAP-PAC-R1-FM SNAP-PAC-R2 SNAP-PAC-R2-FM	96
SNAP-PAC-EB1 SNAP-PAC-EB1-FM SNAP-PAC-EB2 SNAP-PAC-EB2-FM SNAP-PAC-SB1 SNAP-PAC-SB2	96
SNAP-UP1-ADS SNAP-UP1-M64	32
SNAP-B3000-ENET SNAP-ENET-RTC	16

NOTE: PID capabilities in these I/O units are compatible with PAC Control, but not with OptoControl.

The simplest way to use these PIDs is with PAC Control, which provides easy-to-use configuration and tuning tools. For more information, see the *PAC Control User's Guide* (form 1700).

If you are not using PAC Control, however, it is possible to configure and tune PIDs through the I/O unit's memory map. Memory map addresses start on page 81.

You can configure each PID loop with unique settings for a large number of parameters. For a simple PID loop, you must configure at least the following:

- Input (the process variable being monitored)
- Setpoint (the desired value)
- Output (the I/O channel that effects change in the system)
- Scan time (how often the input is sampled, the calculation performed, and the output updated)
- PID algorithm used (Four algorithms are available; see "Algorithm Choices," below.)

You can also configure the following parameters:

- Valid range for input
- Upper and lower clamps for output
- Minimum and maximum change for output
- Forced output value or use of manual mode if input goes out of range
- Feed forward gain
- Square root of input (typically used with differential pressure cells)

In these PID loops, the derivative is applied only to the process variable (the input) and not to the setpoint. This means you can change the setpoint without causing spikes in the derivative term. Non-velocity PIDs also prevent integral windup by back calculating the integral without the derivative term. The feed forward term ("bias") is added before output clamping and has a tuning factor.

If desired, you can cascade PIDs by simply using the output channel of one PID loop as the input channel for another.

PAC-R
EB
SB
UIO
EIO

Algorithm Choices

(Does not apply to *groov* I/O units or *groov* RIO modules.) When you configure a PID loop, choose one of these algorithms[4]:

- Velocity (Type C)
- ISA
- Parallel
- Interacting

Velocity (Type C) is typically used to perform velocity control. The ISA, Parallel, and Interacting algorithms are derived from the article "A Comparison of PID Control Algorithms" by John P. Gerry in *Control Engineering* (March 1987). These three equations are the same except for the tuning coefficients; converting from one equation to another is merely a matter of converting the tuning coefficients.

Key to Terms Used in Equations

`PV`	Process variable; the input to the PID
`SP`	Setpoint
`InLo`, `InHi`	Range of the input
`OutLo`, `OutHi`	Range of the output
`Gain`	Proportional tuning parameter. Unitless. May be negative.
`TuneI`	Integral tuning parameter. In units of seconds. Increasing magnitude increases influence on output.

`TuneD`	Derivative tuning parameter. In units of seconds. Increasing magnitude increases influence on output.
`Output`	Output from the PID
`Err_1`	The Error (PV – SP) from the previous scan
`Integral`	Integrator. Anti-windup is applied after the output is determined to be within bounds.
`PV1, PV2`	PV from the previous scan and the scan before that.
`ScanTime`	Actual scan time (time since previous scan)

Equations Common to All Algorithms

```
Err = PV - SP
Span = (OutHi - OutLo) / (InHi - InLo)
Output = Output + FeedForward * TuneFF
```

Equations Common to ISA, Parallel, and Interacting

```
Integral = Integral + Err
TermP = Err
TermI = TuneI * ScanTime * Integral
TermD = (TuneD / ScanTime) * ( PV - PV1 )
```

Velocity (Type C) Algorithm

```
ΔTermP = ( PV - PV1 )
```

In this part of the formula, you adjust ***Tunel****.*

```
ΔTermI = TuneI * ScanTime * Err
```

---

[4]The following obsolete algorithms support PID loops configured before PAC Project R9.5. For details, see the Opto 22 KnowledgeBase article KB82058

- Velocity (Type B) Obsolete
- ISA (Obsolete)
- Parallel (Obsolete)
- Interacting (Obsolete)

You can continue to use these obsolete algorithms, but Opto 22 recommends you use the new algorithms when configuring new PID loops.

*In this part of the formula, you adjust **TuneD**.*

```
ΔTermD = TuneD / ScanTime * ( PV - 2 * PV1 + PV2 )
```

*In this part of the formula, you adjust **Gain**.*

```
ΔOutput = Span * Gain * ( ΔTermP + ΔTermI + ΔTermD )
```

ISA (or "Ideal") Algorithm

```
Output = Span * Gain * ( TermP + TermI + TermD )
```

Parallel (or "Independent") Algorithm

```
Output = Span * ( Gain * TermP + TermI + TermD )
```

Interacting (or "Classic") Algorithm

```
Output = Span * Gain * ( TermP + TermI ) * ( 1 + TermD )
```

FORMATTING AND INTERPRETING DATA

Data is formatted differently for different addresses in the memory map. The memory map tables in Appendix A (page 81) show whether the data in each address is a mask, a signed or unsigned integer, a float, and so on. This section shows how to format and interpret various types of data when you are reading or writing to a memory-mapped device.

Mask Data

Some data is in the form of a 32-bit or 64-bit mask—four or eight addresses, each holding eight bits. Each bit in the mask contains the data for one thing in a group: one channel, one module, one Scratch Pad bit, etc.

Mask Data for *groov* and SNAP I/O units

For example, most high-density digital module data (for both *groov* and SNAP) and most SNAP digital bank data is in this form (*groov* I/O units and groov RIO modules do not support banks). For example, to read the state of SNAP digital channels in a bank, you would read the eight bytes starting at FFFFF0400000.

Here's how the data would be returned:

At address:	FFFFF0400000								→	FFFFF0400007							
These bit numbers:	7	6	5	4	3	2	1	0	→	7	6	5	4	3	2	1	0
Show data for these points:	3	2	1	0	3	2	1	0	→	3	2	1	0	3	2	1	0
On SNAP modules in these positions in the rack:	15				14				→	1				0			

Therefore, at address FFFFF0400000:

This hex data:	B				1			
Equals this binary data:	1	0	1	1	0	0	0	1
Showing the states:	On	Off	On	On	Off	Off	Off	On
Of these channels:	3	2	1	0	3	2	1	0
On these modules:	15				14			

Data from other addresses marked as masks is formatted in a similar way.

Mask Data for E1s

The bank area of the memory map is based on a four-channel SNAP module. For I/O units with E1 brain boards, each channel is treated as the first channel on a SNAP module. That means that when you read a bank of digital channels on an E1, data appears only in the first of every four channels, like this:

At address:	FFFFF0400000								→	FFFFF0400007							
These bit numbers:	7	6	5	4	3	2	1	0	→	7	6	5	4	3	2	1	0
Show data for these points:	--	--	--	0	--	--	--	0	→	--	--	--	0	--	--	--	0
On G1 or G4 modules in these positions in the rack:	15				14				→	1				0			

So, at address FFFF04000000:

This hex data:	1				0			
Equals this binary data:	0	0	0	1	0	0	0	0
Showing the states:	--	--	--	On	--	--	--	Off
Of these channels:	--	--	--	0	--	--	--	0
On these modules:				1				0

These memory map addresses apply not only to G1 and G4 modules, but also to integral racks and even to Quad Pak modules. Channels on all E1 I/O units are treated the same way, no matter how they are physically placed on the rack.

Unsigned 32-bit Integer Data

Much of the data in the memory map is in the form of unsigned integers, either one byte, two bytes, or four bytes. With multiple bytes, since the memory-mapped devices use a Big Endian architecture, the high order byte is in the low order address.

For example, SNAP digital bank counter data is in 4-byte unsigned integers. It takes four bytes to contain the data for one channel. To read digital bank counter data for channel 0 on module 0, you would start with address FFFFF0400100. The following table shows the pattern of bank counter data for the first few channels on a SNAP rack:

Bytes at these addresses:	FFFFF0400100 FFFFF0400101 FFFFF0400102 FFFFF0400103	FFFFF0400104 FFFFF0400105 FFFFF0400106 FFFFF0400107	FFFFF0400108 FFFFF0400109 FFFFF040010A FFFFF040010B	FFFFF040010C FFFFF040010D FFFFF040010E FFFFF040010F	FFFFF0400110 FFFFF0400111 FFFFF0400112 FFFFF0400113	FFFFF0400114 FFFFF0400115 FFFFF0400116 FFFFF0400117	→
Show data for this point:	0	1	2	3	0	1	→
On the module in this position on the rack:	0				1		→

The most significant byte is at the lowest address. For module 0, channel 0, for example, you might receive the following data:

At this address	This binary data	Equals this hex data	16	BB	18	87
FFFF F040 0100	0001 0110	16				
FFFF F040 0101	1011 1011	BB				
FFFF F040 0102	0001 1000	18				
FFFF F040 0103	1000 0111	87				

The 32-bit integer for this reading would be 16 BB 18 87 (most significant byte at lowest address). This hex figure correlates to the decimal value 381,360,263.

Remember that if you are processing this data using a Little Endian computer (such as an Intel-based PC), you must convert the data from the Big Endian format in order to use it. Little Endian format is the opposite of Big Endian; Little Endian places the most significant byte at the highest address.

Digital Channel Data (4-Channel Modules)

NOTE: For high-density digital modules, see "Mask Data" on page 58.

(Does not apply to *groov* I/O or *groov* RIO modules, which have more than 4 channels.) For consistency in starting addresses, data for individual digital channels has a length of four bytes. However, only the least significant bit contains the data you're looking for.

For example, to read the state of channel 0 on module 0, you would start with address FFFFF0800000. Data would be returned as follows:

To read this information:	Point 0 on Module 0: Point State							
Use these addresses:	FFFFF0800000		FFFFF0800001		FFFFF0800002		FFFFF0800003	
These bits:	7 6 5 4 3 2 1 0		7 6 5 4 3 2 1 0		7 6 5 4 3 2 1 0		7 6 5 4 3 2 1 0	
Contain this data (binary):	0 0 0 0 0 0 0 0		0 0 0 0 0 0 0 0		0 0 0 0 0 0 0 0		0 0 0 0 0 0 0 1	
(hex):	0	0	0	0	0	0	0	1
	Ignore these						Point state is ON.	

Digital Channel Data for E1s

If you are using I/O units with E1 brain boards, remember that the memory map is based on a four-channel SNAP module. For an E1, channel data appears in the addresses that correspond to the first of each group of four channels in the memory map, like this:

Addresses for point state:	FFFFF0800F00	FFFFF0800E00	FFFFF0800D00	FFFFF0800C00	FFFFF0800B00	FFFFF0800A00	FFFFF0800900	FFFFF0800800	FFFFF0800700	FFFFF0800600	FFFFF0800500	FFFFF0800400	FFFFF0800300	FFFFF0800200	FFFFF0800100	FFFFF0800000
E1 module position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Point number:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Channel data appears this way for all module types used with an E1: G1, G4, Quad Pak, and integral racks.

IEEE Float Data

For individual analog channels, values, counts, and minimum and maximum values for one channel are located next to each other in the memory map. All are four bytes and are IEEE 754 floats.

For example, individual analog channel data for channels 0 and 1 on module 0 appears in these addresses:

Module	Channel	Data	Beginning Address	Ending Address
0	0	Scaled units (E.U.*)	FFFF F026 0000	FFFF F026 0003
		Counts	FFFF F026 0004	FFFF F026 0007
		Minimum value (E.U.*)	FFFF F026 0008	FFFF F026 000B
		Maximum value (E.U.*)	FFFF F026 000C	FFFF F026 000F
	1	Scaled units (E.U.*)	FFFF F026 0040	FFFF F026 0043
		Counts	FFFF F026 0044	FFFF F026 0047
		Minimum value (E.U.*)	FFFF F026 0048	FFFF F026 004B
		Maximum value (E.U.*)	FFFF F026 004C	FFFF F026 004F

* Engineering Units

IEEE 754 float format is as follows:

1 bit	8 bits	23 bits
x	xxxxxxxx	xxxxxxxxxxxxxxxxxxxxxxx
Sign	Exponent	Significand

Float calculation: $(-1)^{Sign} \times [1 + Significand/2^{23}] \times 2^{(Exponent-127)}$

Example for Opto 22 memory map

At this address:	base address		base address + 1		base address + 2		base address + 3	
This hex data:	41		77		33		33	
In binary:	0	100 0001	0	111 0111	0011	0011	0011	0011
In these bits:	31	30 . . . 23	22 . . . 0					
Equals (in decimal):	0	130	7,811,891					
Representing:	Sign	Exponent	Significand					

Decimal $= (-1)^{0} \times [1 + 7{,}811{,}891/2^{23}] \times 2^{(130-127)}$

$= 1 \times [1.931] \times 8$

$= 15.45$ (rounded to 2 decimal places)

For more information on floats and issues that may arise in their use, see the Using Floats Technical Note (form 1755) available on our website, www.opto22.com.

Analog Bank Data

(Does not apply to *groov* I/O units or *groov* RIO modules.) Remember that the bank area of the memory map is set up for four channels per module. Analog modules with more than four channels (points) will show data for channels 0–3 only. If the analog modules you are using have only one or two channels, the addresses for the upper two or three channels in each module will contain the following: for output modules, 0; for input modules, FFFFFFFF.

For example, to read all bank analog channel values in scaled units, you would read 256 bytes starting at address FFFFF0600000. Here's how data for two-channel input modules in positions 0 and 1 would appear:

Beginning Address	Ending Address	Data Format	Module	Channel
FFFF F060 0000	FFFF F060 0003	four bytes—IEEE float	0	0
FFFF F060 0004	FFFF F060 0007	four bytes—IEEE float		1
FFFF F060 0008	FFFF F060 000B	FFFFFFFF		2
FFFF F060 000C	FFFF F060 000F	FFFFFFFF		3
FFFF F060 0010	FFFF F060 0013	four bytes—IEEE float	1	0
FFFF F060 0014	FFFF F060 0017	four bytes—IEEE float		1
FFFF F060 0018	FFFF F060 001B	FFFFFFFF		2
FFFF F060 001C	FFFF F060 001F	FFFFFFFF		3

On an I/O unit with an E2 brain board, all modules have only one channel, so the upper three channels would contain 0 (outputs) or FFFFFFFF (inputs).

3: Using OptoMMP Software Development Kits

INTRODUCTION

Opto 22 provides two free software development kits (SDKs) for communication between a computer and an Opto 22 Ethernet-based memory-mapped device: one for C++ running under Windows or Linux, and the other for .NET environments.

Both are available for download from our website at www.opto22.com.

These SDKs provide an interface so you can access Opto 22 memory-mapped devices through your custom software application without having to understand the details of the OptoMMP protocol.

Both kits include complete API documentation, source code, and examples.

Many resources—courses, books, and online materials—are available for learning how to program in these languages. SDK documentation assumes that you already know how to program in the language of your choice.

For both SDKs, see Chapter 2: Overview of Programming for basic information about Opto 22 hardware and features, and Appendix A: Opto 22 Hardware Memory Map for all memory map addresses.

C++ OPTOMMP SOFTWARE DEVELOPMENT KIT FOR *groov* EPIC, *groov* RIO, AND SNAP PAC

The C++ OptoMMP Software Development Kit for *groov* EPIC, *groov* RIO, and SNAP PAC, part number PAC-DEV-OPTOMMP-CPLUS, contains C++ source code that you can link into your custom application. Use this SDK if you are on Windows or Linux and want to write your own C++ program to read or write to *groov* EPIC processors, *groov* RIO modules, or SNAP PAC controllers or brains.

To use this SDK:

1. Download it from www.opto22.com: PAC-DEV-OPTOMMP-CPLUS
2. Unzip the file.
3. In the extracted files, find the Docs folder, and then double-click the index.html file to open it in a web browser. Choose Classes > Class Members > Functions to see documentation on all the functions.

A Few Examples

Here are a few examples of reading and writing to channels with the C++ SDK. Notice that chassis (rack) positions and channels (points) on modules are zero-based. See "Referencing Module and Channel Positions on I/O Units" on page 9.

Read the value of channel 17 on an analog input module in position 1 on the rack (the second position; first position is position 0).

- Use function: GetAnalogPointValueEx
- nModule is 1
- nPoint is 17

Write analog output 13 on module in position 3 on the rack.

- Use function: SetAnalogPointValueEx
- nModule is 3
- nPoint is 13

Read analog channel 2 on module in position 2 on the rack:

- Use function: GetAnalogPointValueEx
- nModule is 2
- nPoint is 2

Read high-density digital (HDD) input channel 4 on module in position 5 on the rack:

- Use function: GetHDDigitalPointState
- nModule is 5
- nPoint is 4

Write to HDD output channel 3 on module in position 3 on the rack:

- Use function: SetHDDigitalPointState
- nModule is 3

Write to standard 4-channel digital output channel 1 in module position 7:

- Use function: SetDigPtState
- nPoint is 29 (7x4 + 1 = 29. Remember that channel 1 is the second channel on the module.)

Read 4-channel digital input channel 2 in module position 8:

- Use function: GetDigPtState
- nPoint will be 34 (8x4 + 2 = 34)

.NET OPTOMMP SOFTWARE DEVELOPMENT KIT FOR *groov* EPIC, *groov* RIO, AND SNAP PAC

The .NET OptoMMP Software Development Kit for *groov* EPIC, *groov* RIO, and SNAP PAC, part number PAC-DEV-OPTOMMP-DOTNET, contains a .NET DLL that you add as a reference in your .NET program. Use this SDK if you are creating a .NET application on Windows.

To use this SDK:

1. Download it from www.opto22.com: PAC-DEV-OPTOMMP-DOTNET
2. Unzip the file.
3. Open the Documentation folder and double-click the index.html file to open documentation in a web browser.
4. Read the short .NET OptoMMP SDK for *groov* EPIC and SNAP PAC technical note (form 2135) to get started.

4: Using the OptoMMP Protocol

INTRODUCTION

This chapter shows you how to use the OptoMMP protocol to write your own applications for direct communication between a PC and an Opto 22 Ethernet-based memory-mapped device, for example, if you are writing your own driver. [1]

This chapter assumes the following:

- Your Ethernet network—including a PC, hubs if needed, and one or more Opto 22 devices—is already installed. (For help installing and troubleshooting your hardware, see the user's guides listed on page 3.)
- Unique, appropriate IP addresses have been assigned to the devices.
- Each device can be reached by the host PC using the PING program.

This chapter also assumes that you are familiar with programming, TCP/IP or UDP/IP, and Ethernet networking. If you are not familiar with these subjects, we strongly suggest you consult commercially available resources to learn about them before attempting to program applications for memory-mapped hardware.

The complete memory map is in Appendix A, starting on page 81. This memory map covers all possible addresses; some may not apply to the hardware you are using. For detailed information on hardware models and features, see the Appendix C: SNAP Features Comparison Chart.

[1] To quick start your development process, try our SDKs for Microsoft Windows and Linux platforms. For details, see Chapter 4: Using the OptoMMP Protocol.

MEMORY MAPPING

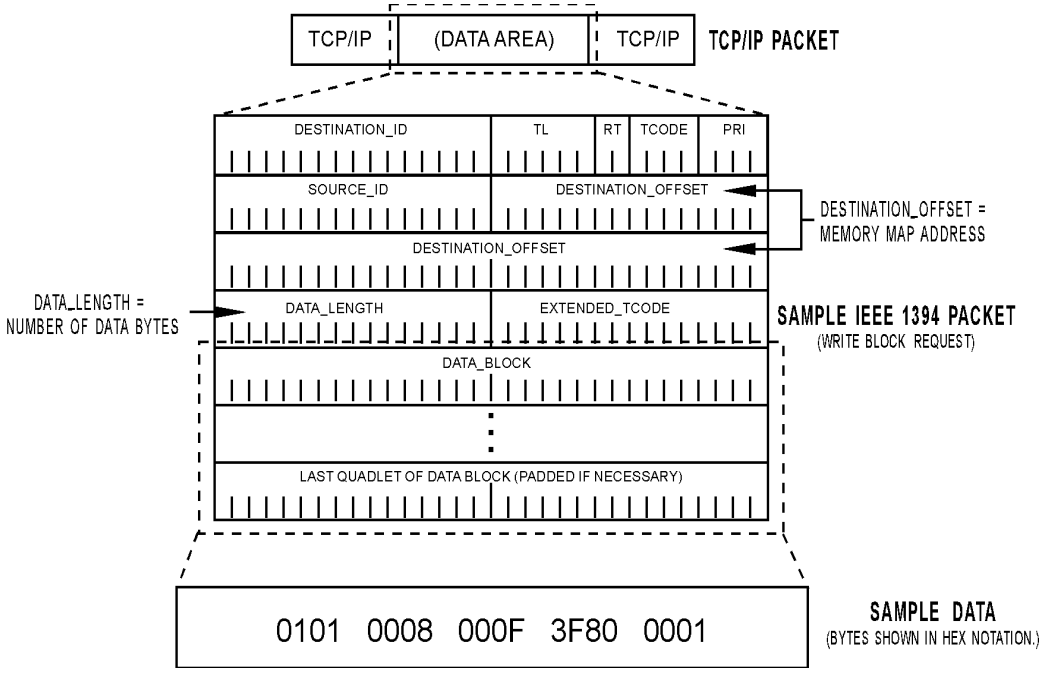
PR1
RIO
PAC-R
PAC-S
EB
UIO
EIO
SIO
LCE
E1
E2

Opto 22 memory-mapped devices use the OptoMMP protocol, based on the IEEE 1394 specification, to provide a standard for reading and writing data.

IEEE 1394 specifies a memory-mapped model for devices on a serial network. For asynchronous transfers, it also specifies a request-response protocol for read/write operations. Basically, each IEEE 1394 node appears logically as a 48-bit address space. To communicate with a device, you read from and write to specific memory addresses in that space. See Appendix A: Opto 22 Hardware Memory Map for memory map addresses.

Communication Packets

Communication using the OptoMMP protocol basically involves an IEEE 1394 packet placed inside a TCP/IP or UDP/IP packet. These nested packets look like this TCP example:



The Opto 22 memory-mapped device uses the following types of request packets specified by the IEEE 1394 standard:

- Read Quadlet: reads four bytes starting at an address
- Read Block: reads N bytes starting at an address
- Write Quadlet: writes four bytes starting at an address
- Write Block: writes N bytes starting at an address.

To start communication with the memory-mapped device, the host computer sends one of these four packets via TCP/IP or UDP/IP. To complete each transaction, the device returns a Read Response packet or a Write Response packet. The structure and parameters of the request and response packets are shown beginning on page 76.

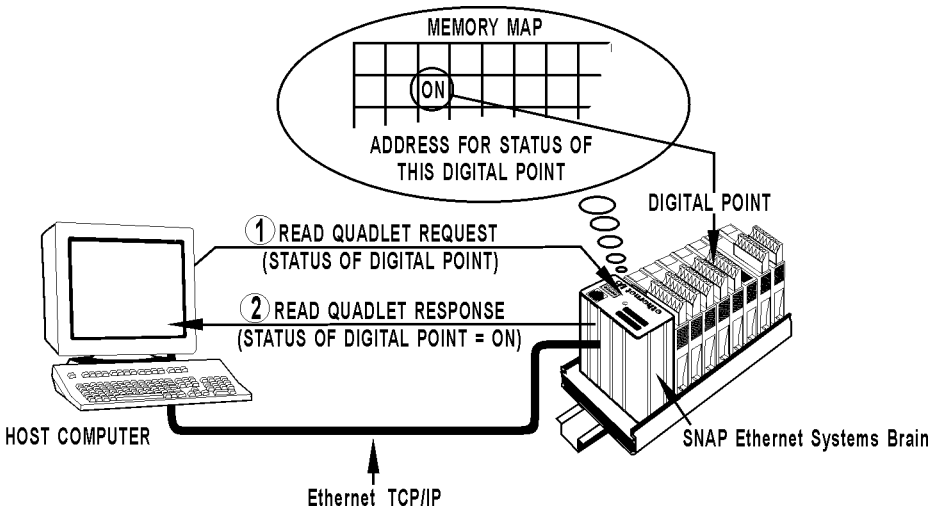
Writing Data

To change the configuration or status of an I/O channel, to enable a counter, or to write other data, the host sends a Write Request packet containing the destination address and the new data to be written. The device responds by returning a Write Response packet indicating success or failure.

Reading Data

The host can also access the status of I/O modules, counter values, and other data by reading the appropriate memory locations from the memory map. The host computer simply sends a Read Request packet asking for data from those memory locations, and the device returns the data in a Read Response packet.

The following diagram shows a specific example of a host computer reading data from a SNAP Ethernet-based I/O unit:



Streaming Data

Most communication involves the two-step process of request and response. But some Opto 22 memory-mapped devices can also stream data, as explained on page 51. Streaming uses UDP and does not require a response.

For more information on using streaming, see page 72.

OVERVIEW OF CUSTOM APPLICATION PROGRAMMING

PR1
RIO
PAC-R
PAC-S
EB
UIO
EIO
SIO
LCE
E1
E2

If you are not using either of the OptoMMP software development kits (SDKs) described on page 63 but need to develop custom applications using the protocol itself, this section shows you how to build packets to communicate with Opto 22 memory-mapped hardware.

Programming requires five basic steps: connect, send Powerup Clear, configure, read/write, and disconnect. This overview section leads you through these steps.

Connecting

To connect with the device, you can use a basic socket interface, such as Microsoft Winsock control. Assign the IP address and port. Note that the OptoMMP port defaults to 2001 for the device (You can change this port number using address F03A0004 (see page 104). If the variable name for the device is tcpIOUnit, the connection would look like this:

```
tcpIOUnit.RemoteHost = "10.192.0.69" 'IP address of device
tcpIOUnit.RemotePort = 2001
tcpIOUnit.Connect
```

Sending Powerup Clear

Once a connection has been established, the host must send a Powerup Clear message (PUC) to the memory-mapped device. You can't do anything except read the memory map's Status area until the Powerup Clear is sent. Other requests will return a negative acknowledgment (NAK), and the error Powerup Clear Expected will appear in the Status area. (See page 101.)

After the initial PUC is sent, you do not need to send another unless the device has been turned off or restarted. To check whether a Powerup Clear is needed, you can read the PUC flag in the Status area. A zero means the PUC has been sent; anything else means you must send a PUC.

To send a Powerup Clear, build a Write Quadlet Request packet with data 00000001 written to offset FFFFF0380000, which is the memory map location for sending a Powerup Clear. (The complete memory map is shown in Appendix A, starting on page 81.)

Write Quadlet Request Packet (from PC to Device)

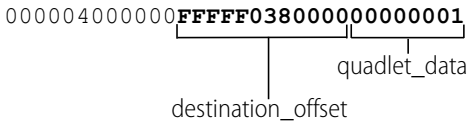
In binary notation, the packet is organized as follows:

	destination_ID																tl						rt		tcode				pri			
Bytes 0–3 →	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	source_ID																destination_offset															
Bytes 4–7 →	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	destination_offset																															
Bytes 8–11 →	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	quadlet_data																															
Bytes 12–15 →	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Converted to hexademical, the same packet looks as follows:

	destination_ID				tl		rt	tcode	pri
Bytes 0–3 →	0	0	0	0	0	4		0	0
	source_ID				destination_offset				
Bytes 4–7 →	0	0	0	0	F	F	F	F	
	destination_offset								
Bytes 8–11 →	F	0	3	8	0	0	0	0	
	quadlet_data								
Bytes 12–15 →	0	0	0	0	0	0	0	1	

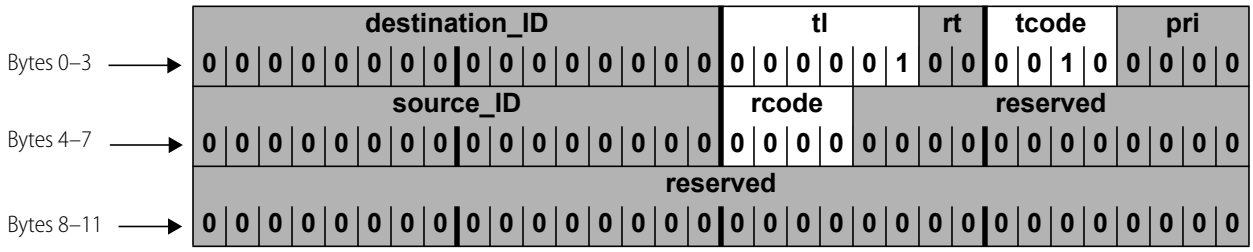
Written in one long hex string, the packet looks like this:



For more information on communication packets, see "Read and Write Packet Structure" on page 76.

Write Response Packet (from Device to PC)

When the device receives the Powerup Clear, it sends a Write Response packet back to the host PC acknowledging receipt. In binary notation, the response packet looks like this:



The *rcode* parameter contains the ACK or NAK for the transaction. The 0 in this example indicates an ACK.

In hex, the packet looks like this: `000004200000`**`0`**`00000000000`. The `0` shown in bold type is the ACK in the *rcode*.

See "Error Codes" on page 80 for information on what to do if you receive a NAK.

Configuring

SNAP Ethernet-based I/O units (but not E2 I/O units) can recognize the presence and type of an analog module on the rack, but the values for each of the channels must be configured if they do not match the default for that module type. For example, the I/O unit can report that a SNAP-AITM module is in position 4, but if the channels are anything other than the default value of ±150 mV, you must configure them by writing configuration codes to the channels.

- *groov* I/O unit module types, channel types, and default values are shown in the tables starting on page 16.
- SNAP module types, channel types, and default values are shown in the tables starting on page 21.

Digital modules and empty positions are reported the same by an Ethernet-based I/O unit or an E1 I/O unit: they are assumed to be digital input modules. If a position contains a digital output module, you must configure the channels as outputs.

Serial and high-density digital modules do not require configuration for use with custom applications.

Configuring I/O Channel Types—Write Quadlet Request Packet (from PC to Device)

Suppose you have a digital output module in position 0 on the rack. Since the I/O unit cannot distinguish a digital module from an empty position, you need to configure the channels (for a SNAP module, all channels) as outputs. You configure them by writing to each one's Channel Type address in the "(Expanded) Analog & Digital Channel Configuration—Read/Write" area of the memory map. On page 85 you can see this area of the map.

The Write Quadlet Request for channel 0 would look like this: `000004000000FFFF`**`F0100004`**`00000180`

Write Quadlet Request for channel 1 (hex): `000004000000FFFF`**`F01000C4`**`00000180`

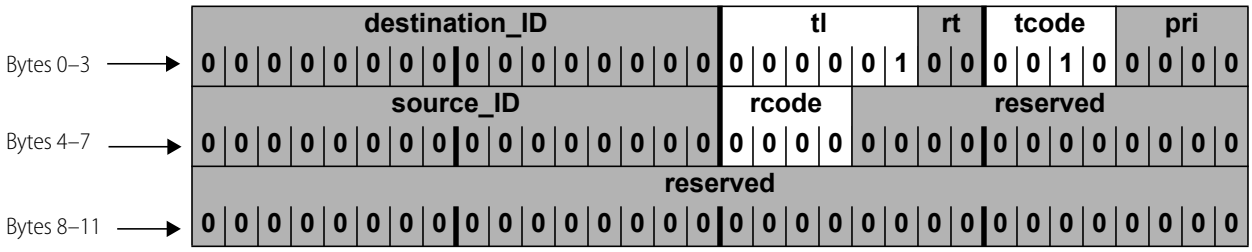
Write Quadlet Request for channel 2 (hex): `000004000000FFFF`**`F0100184`**`00000180`

Write Quadlet Request for channel 3 (hex): `000004000000FFFF`**`F0100244`**`00000180`

As you can see, the only difference in these packets is the memory map address for the channel. For more information on module types and setting channel types, see "Configuring I/O Channels and Features" on page 72.

Configuring I/O Channel Types—Write Response Packet (from Device to PC)

The response from the device is a simple acknowledgment, as you saw before, with the ACK or NAK appearing in the *rcode* parameter:



Reading and Writing

Now that the PC has successfully connected to the device, sent a Powerup Clear, and configured I/O channels as necessary, you can read and write to the channels.

Turn on Digital Channels—Write Block Request (from PC to Device)

Suppose you want to turn on multiple channels on 4-channel digital modules. Using bank addresses in the memory map, you can turn them on all at once. As you can see on page 120, the starting address for Turn On (Digital Bank Write) is `FFFFF0500000`. This starting address goes into the *destination_offset* parameter.

Since this portion of the memory map is a mask, you need to use the entire length of 8 bytes (hex). The length goes into the *data_length* parameter. The *data_block* parameter contains the mask. (For more information on formatting data for a mask, see "Mask Data" on page 58.) The mask shown in this example would turn on channels 1 and 3 on modules 0 and 1, and all four channels on modules 2–7.

Here is the Write Block Request:

In hex, the request would look like this:

000004100000FFFFF0500000000800000000000FFFFFFAA...

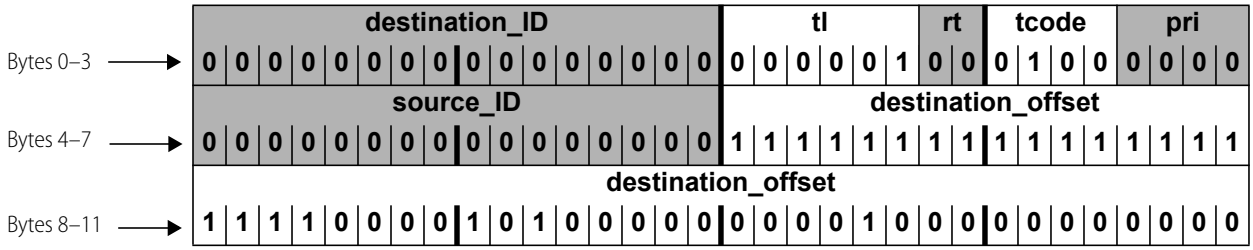
The starting address and the mask are shown in bold.

Turn on Digital Channels—Write Block Response (from Device to PC)

Again, look in the *rcode* parameter of the Write Block Response from the device to see an ACK (0) or a NAK (other than 0).

Read Analog Channel Data—Read Quadlet Request (from PC to Device)

Suppose you want to read the value of channel 1 on module 0, which is an analog channel. You can tell from the memory map ("(Expanded) Analog Channel Read—Read Only" on page 88) that the value in Engineering Units for module 0, channel 1 is at the address FFFFF0260040. The Read Quadlet Request would look like this:

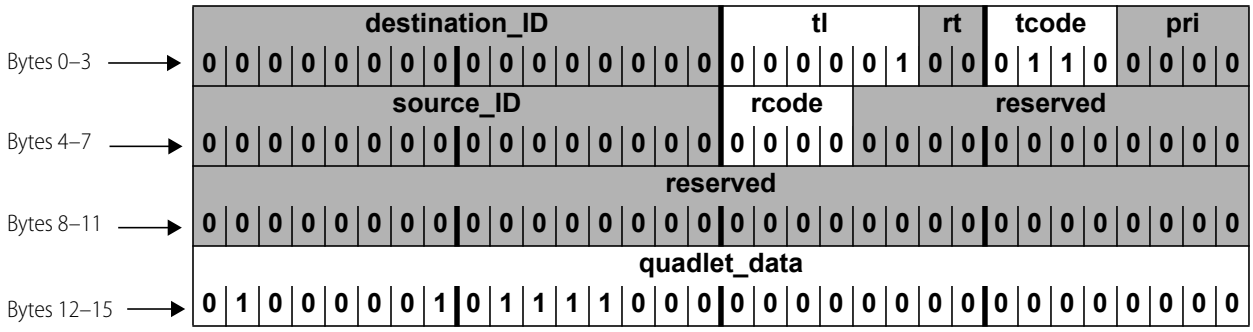


In hex, the request would be as follows (address is bolded):

000004400000**FFFFF0260040**

Read Analog Channel Data—Read Quadlet Response (from Device to PC)

The response to your request might look like this in binary notation:



In hex, it would look like this: 00000460000000000000000041780000

The *rcode* parameter shows an ACK (0), and the *quadlet_data* parameter, shown in bold type in the hex version, equals the IEEE float 15.5.

Disconnecting

The connection is kept open during normal communications. Disconnect only when all communication is complete. To disconnect, you can again use a basic socket interface, such as Microsoft Winsock control:

```
tcpIOUnit.Close
```

STREAMING DATA

PR1
RIO
PAC-R
EB
UIO
EIO
SIO

Streaming is a fast way to get continuous information about I/O from some memory-mapped devices.[2] See page 51 for information on streaming and other methods to configure it. Streaming involves two steps: configuring parameters for streaming, and receiving streamed data.

Note that *groov* EPIC processors and *groov* RIO modules have a built-in firewall. To allow streaming, you'll need to add a rule to allow outgoing communications on the port you want to use for streaming. For instructions to modify firewall rules in *groov* Manage, see the *groov EPIC User's Guide* (form 2267) or the *groov RIO User's Guide* (form 2324).

Configuring Parameters for Streaming

To configure parameters for streaming, use a Write Block Request to the memory map area "Streaming Configuration—Read/Write" on page 119.

- To FFFFF03FFFD4, write how often in milliseconds you want to receive the streamed data.
- To FFFFF03FFFD8, write the Ethernet port number that will receive data.
- To the Stream Target addresses, write the IP addresses of the hosts that should receive the data.
- To turn streaming on, write anything but a zero to the address FFFFF03FFFD0. To turn streaming off, write a zero to this address.

Receiving Streamed Data

As soon as you've configured parameters for streaming, the device starts sending the data you requested. The device sends data using a Write Block Request, with the *data_block* parameter containing data as shown in the memory map area "Streaming—Read Only" on page 138. Your custom application does not need to respond to this Write Block Request; it only needs to process the data block.

Addresses will be zero-filled in areas that don't apply. For example, addresses FFFFF1000000 through FFFFF10000FF show analog data for 64 channels in Engineering Units. If some of the channels are digital, addresses corresponding to them will be filled with zeros.

See "Traditional Stream Packet Format" on page 52 for additional information.

CONFIGURING I/O CHANNELS AND FEATURES

See Chapter 2: Overview of Programming for important information on configuring I/O modules and channels, I/O channel features, event/reactions, and other system functions.

PR1
RIO
PAC-R
EB
UIO
EIO
SIO

Reading Module Types

groov EPIC processors can recognize all *groov* EPIC module types. Empty slots show a channel quality indication of 30 (decimal) indicating no channel present. For *groov* I/O module and channel type values, see page 16.

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[2] If you don't need to stream the data, you can use *Packed Data* areas to get a large amount of data all at once. These areas put large amounts of related data into one area of the memory map so it's faster and easier to read in one transaction. For details, see "(Expanded) Digital Packed Data—Read Only" on page 91, "(Expanded) Digital Packed Must on/OFF (MOMO)—Read/Write" on page 91, "Analog EU or Digital Counter (Feature) Packed Data—Read" on page 139, and "Digital Packed Data—Read/Write" on page 139.

groov RIO is a single module, module type 0xF0000022.

SNAP and other legacy I/O units (analog/digital/serial/mixed) can recognize analog, high-density digital and special-purpose modules on the rack, and can report what their module types. By default, *all SNAP I/O units report 4-channel digital modules (both input and output) and empty slots as digital inputs.* For SNAP I/O module and channel type values, see page 21.

To read a module type, see "(Expanded) Analog & Digital Channel Configuration—Read/Write" on page 85.

PR1
RIO
PAC-R
EB
UIO
EIO
SIO
E1
E2

Configuring I/O Channel Types

Although some I/O units recognize many module types, they may not recognize 4-channel digital modules or individual analog channel values. Also, if the actual module type or channel values differ from the defaults, you must assign the correct values by writing to the "(Expanded) Analog & Digital Channel Configuration—Read/Write" area of the memory map. (See page 85.)

- For *groov* I/O module and channel type values, see page 16.
- For *groov* RIO channel type values, see page 20.
- For SNAP I/O module and channel type values, see page 21.
- To configure I/O channel types, see "Configuring I/O Channels" on page 16.

USING I/O CHANNEL FEATURES

General information on I/O channel features is on page 31. This section provides specific information for the OptoMMP protocol.

PR1
RIO
PAC-R
EB
UIO
EIO
SIO
E1

Latches

Latching is automatic and needs no configuration. Using the Opto 22 protocol, you can read the on-latch or off-latch state of a digital input channel (exception: latches are not available on *groov* simple I/O modules or *groov* RIO simple discrete channels).

You can:

- Read latches for individual channels and leave them set
- Read latches for a bank of digital channels and leave them set
- Read latches for individual channels.

To read latches for individual channels on modules with more than 4 channels, see "High-Density Digital—Read Only" on page 147.

To read latches for individual channels on 4-channel modules, see the memory map area "Digital Channel Read—Read Only" on page 121, and use the on-latch or off-latch state starting address for the channel you want to read. For example, you would read off-latch status for module 0, channel 0 starting at address FFFFF0800002.

To read a bank of channels on 4-channel modules, see the memory map area "Digital Bank Read—Read Only" on page 119. The starting address for reading the state of on-latches is FFFFF0400008, and the starting address for off-latches is FFFFF0400010.

To read latches for individual channels (all digital modules), see the memory map area "(Expanded) Digital Channel Read & Clear—Read Only" on page 90. If you are reading and clearing the on-latch at module 0, channel 1, for example, you would use the starting address FFFFF02E0018. Alternatively, for channels on high-density digital modules, you can latches using "High-Density Digital Read and Clear—Read/Write" on page 147.

For help in understanding the data you read, see "Formatting and Interpreting Data" on page 58.

PR1
RIO
PAC-R
EB
UIO
EIO
E1

Counters

This feature applies to digital input channels on I/O units with the following processors (exception: does not apply to *groov* simple I/O modules or *groov* RIO simple discrete channels.

- GRV-EPIC-PR1
- GRV-R7-MM1001-10
- SNAP-PAC-R1
- E1
- SNAP-UP1-ADS
- SNAP-B3000-ENET
- SNAP-ENET-RTC

When configured, it will count the number of times the input changes from off to on. For most channels, using counters involves two steps: configuring the counter and reading data.

NOTE: On SNAP high-density digital channels, counting is automatic and requires no configuration for use with the OptoMMP protocol.

Configuring a Counter

(Not necessary for SNAP high-density digital channels.) To configure a digital input as a counter, first configure the channel as an input. Write to the "(Expanded) Analog & Digital Channel Configuration—Read/Write" area of the memory map. (See page 85.) For example, to configure module 0, channel 0 as a counter, you would write to the memory map address FFFFF0100004, using 00000100 as the data for a digital input.

Next, configure the channel feature as a counter. In the same area of the memory map, for the same channel, you would write to the address FFFFF0100008 and use 00000001 as the data for a counter.

Reading a Counter

You can:

- Read counters for individual channels and leave them counting
- Read a bank of channels and leave them counting
- Read *and clear* individual channel counters in one step, setting the counters back to zero

For channels on SNAP high-density digital modules, to read counters, see "High-Density Digital—Read Only" on page 147 or "Analog EU or Digital Counter (Feature) Packed Data—Read" on page 139. To read counters, see "High-Density Digital Read and Clear—Read/Write" on page 147.

To read counters for individual channels, see the memory map area "Digital Channel Read—Read Only" on page 121, and use the counter data starting address for the channel you want to read. For example, you would read counter data for module 0, channel 1 starting at address FFFFF0800044.

To read a bank of channels, see the memory map area "Digital Bank Read—Read Only" on page 119. The starting address for reading counter data is FFFFF0400100. For help in interpreting this data, see "Mask Data" on page 58.

To read and clear counters for individual channels on all digital modules, see the memory map area "(Expanded) Digital Channel Read & Clear—Read Only" on page 90. If you are reading and clearing the counter at module 0, channel 0, for example, you would use the starting address FFFFF02E0000.

PR1
PAC-R
EB
SB
UIO
EIO

Quadrature Counters

See page 34 for information on using quadrature counters.

PR1
RIO
PAC-R
EB
UIO
EIO
SIO
E1
E2

Watchdog

Watchdog does not apply to *groov* simple I/O modules or *groov* RIO simple discrete channels.

Using a watchdog involves three steps:

1. Setting up the watchdog time in milliseconds
2. Configuring the watchdog values for the critical channels on digital and analog modules
3. Enabling the watchdog for those channels

Set up the watchdog time by using the "Status Area Write—Read/Write" on page 101. Write the watchdog time in milliseconds starting at the address FFFFF0380010. This is the amount of time the I/O unit will wait for communication from the host device.

Configure the watchdog values for digital and analog channels using the memory map area "(Expanded) Analog & Digital Channel Configuration—Read/Write" on page 85. These are channels you want to set to a certain state or value if the watchdog timeout occurs. For example, to close a valve at digital output channel 1 on module 0, you would write a zero starting at the address FFFFF0100024. To set a value on analog output channel 0 on module 1, you would write the EU float starting at the address FFFFF01000E4.

Enable the watchdog for the channels for which you've set watchdog values, also using "(Expanded) Analog & Digital Channel Configuration—Read/Write" on page 85. For the example of the digital output at channel 1, you would write starting with the address FFFFF0100028. For the analog output at channel 4, the starting address would be FFFFF01000E8.

PR1
RIO
PAC-R
EB
UIO
EIO
SIO
E2

Scaling

Scaling applies to analog channels only. To scale a channel, see the memory map area "(Expanded) Analog & Digital Channel Configuration—Read/Write" on page 85. Write to the channel's addresses for high scale and for low scale. For example, to scale module 0, channel 0, you would write the high-scale float starting at the address FFFFF0100014 and the low-scale float starting at FFFFF0100018.

PR1
RIO
PAC-R
EB
UIO
EIO
SIO
E2

Minimum and Maximum Values

Memory-mapped I/O units with analog capability automatically keep track of minimum and maximum values on analog channels. You can read the values at any time, for example, to record minimum and maximum temperatures. You can:

- Read min/max values for individual channels
- Read a bank of channels
- Read *and restart* min/max values for individual channels

To read min/max values for individual channels, see the memory map area "(Expanded) Analog Channel Read—Read Only" on page 88, and use the Min Value or Max Value starting address for the channel you want to read. For example, you would read the minimum value for module 0, channel 0 starting at address FFFFF0260008.

To read min/max values for a bank of channels, see the memory map area "Analog Bank Read—Read Only" on page 120. The starting address for reading minimum values is FFFFF0600200. For help in interpreting this data, see "IEEE Float Data" on page 61.

To read and restart min/max values for individual channels, see the memory map area "(Expanded) Analog Channel Read & Clear—Read/Write" on page 87. For example, if you want to record the maximum temperature at module 0, channel 1 in each 24-hour period, the values must be reset when they are read each

day. You would read and restart the maximum value for module 0, channel 0 using the starting address FFFFF01D4010.

PR1
RIO
PAC-R
EB
UIO
EIO
SIO
E2

Offset/Gain

Offset and gain apply to analog input channels only. To have the I/O unit calculate offset and gain, use the memory map area "(Expanded) Analog Channel Calc & Set—Read/Write" on page 87. Calculate offset first, then calculate gain.

For example, calculate offset for module 0, channel 1 by reading addresses FFFFF01C0008 through FFFFF01C000B. Calculations are completed in the background, and the response gives the offset in counts. Next, calculate gain for the same channel by reading addresses FFFFF01C000C through FFFFF01C000F. Response for gain is in percent.

Since the purpose of the read request is simply to have the offset or gain calculated so that values you read later will be accurate, you can normally ignore the response data.

If you want to save the response data—or if you want to calculate offset and gain by hand—you can write this data to the memory map area "(Expanded) Analog & Digital Channel Configuration—Read/Write" on page 85.

READ AND WRITE PACKET STRUCTURE

Parameters

The following table defines the parameters for all requests and responses:

Parameter	Full Name	Description
destination_id	Destination identifier	Not used by Opto 22 memory-mapped devices. Set this parameter to zero.
tl	Transaction label	A label specified by the requester and identifying this transaction. This value is returned in the response packet.
rt	Retry code	Not used by Opto 22 memory-mapped devices. Set this parameter to zero.
tcode	Transaction code	Defines the type of packet: Write Quadlet Request = 0 Write Block Request = 1 Write Quadlet or Block Response = 2 Read Quadlet Request = 4 Read Block Request = 5 Read Quadlet Response = 6 Read Block Response = 7
pri	Priority	Not used by Opto 22 memory-mapped devices. Set this parameter to zero.
source_id	Source identifier	Optional parameter. If you are running two or more applications simultaneously, you can give each application a different ID in this parameter. If an error occurs, you can read the Source address in the memory map Status area to find out which application caused the error. See page 92.
rcode	Response code	Indicates whether the command was successful. Successful command (ACK) = 0 Unsuccessful command (NAK) = any number except zero. If you receive a NAK in this parameter, see "Error Codes" on page 80.

Parameter	Full Name	Description
destination_offset	Destination offset	Specifies the address location in the target node.
data_length	Data length	Specifies the amount of data being sent in the data parameter of this packet. Maximum size is 2034 bytes for data sent via TCP, or 1480 bytes for data sent via UDP.
extended_tcode	Extended transaction code	Not used by Opto 22 memory-mapped devices. Set this parameter to zero.
quadlet_data	Quadlet data	Data being delivered to the target node. If it is not an even four bytes of data, pad with zeros at the end, not the beginning.
data_block	Data parameter	Data being transferred to the target device.

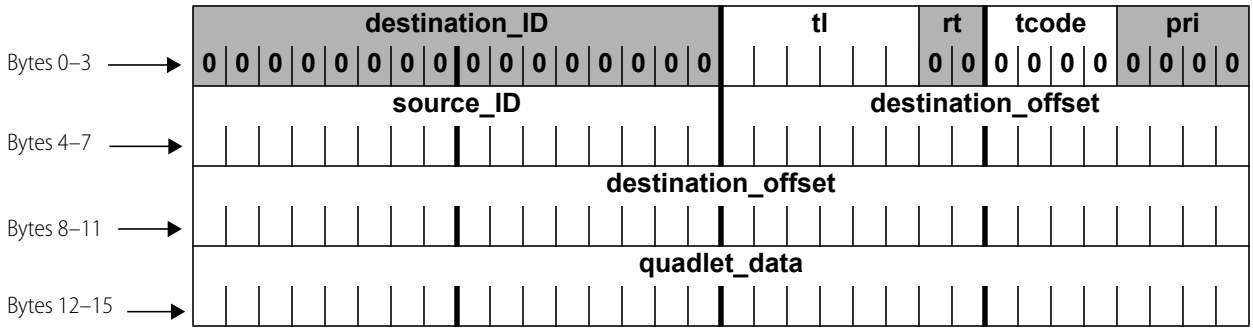
Packet Structure

The following pages show the structure for read and write request and response packets. Opto 22 memory-mapped devices do not use the parameters *destination_ID, rt,* or *pri* (or *reserved* areas). These areas must be zero filled. They are shown shaded. The *source_ID* parameter (described in the previous table) is optional. If you do not use it, fill it with zeros.

OptoMMP packets have boundaries at four bytes (a quadlet). When you send a Write Quadlet Request, if the data you enter in the *quadlet_data* parameter is less than four bytes, fill the remaining spaces with zeros to complete the quadlet. Zero fill at the end, not the beginning, of the data.

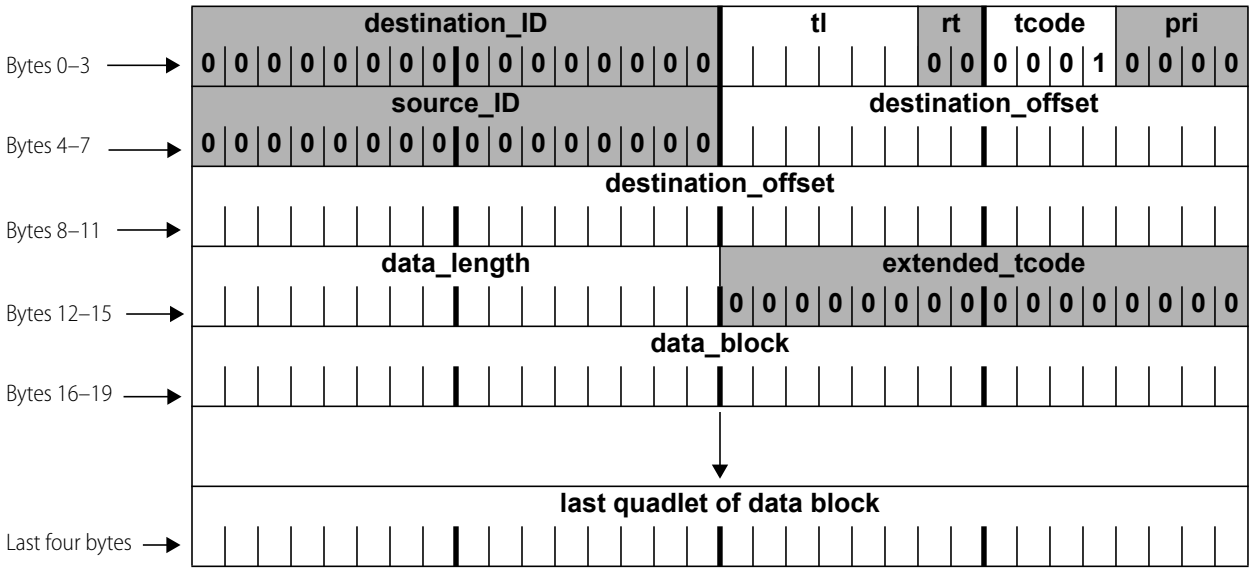
Write Quadlet Request

Tcode = 0



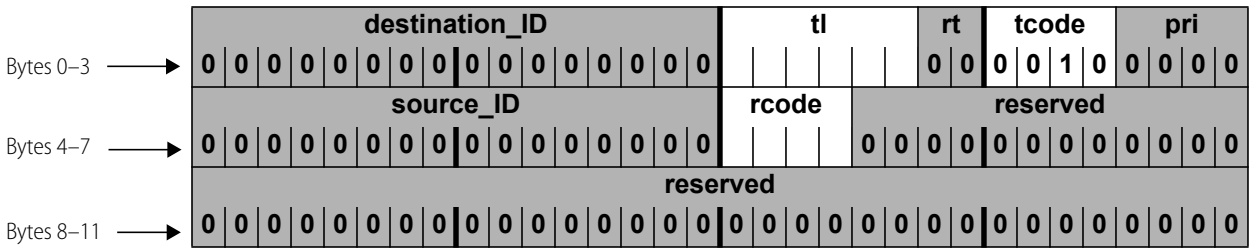
Write Block Request

Tcode = 1



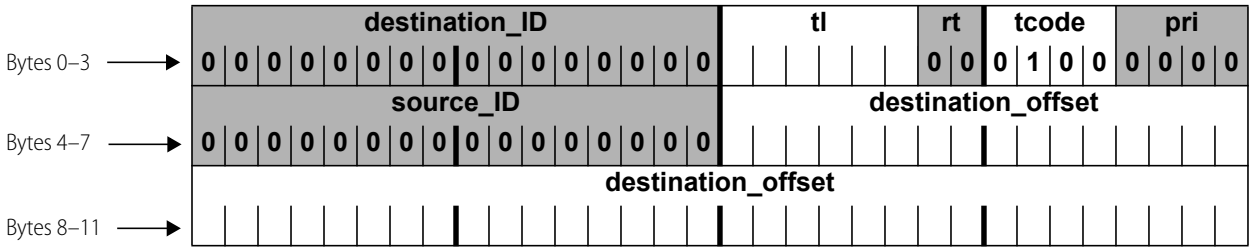
Write Quadlet or Block Response

T-code = 2



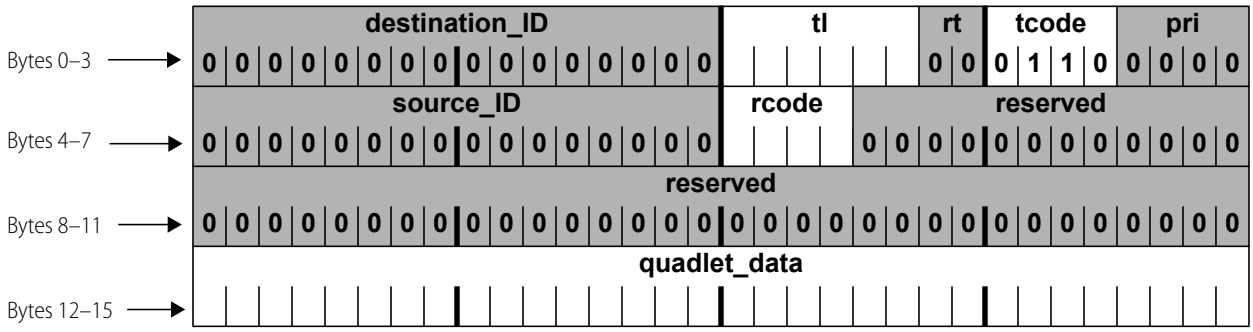
Read Quadlet Request

Tcode = 4



Read Quadlet Response

Tcode = 6

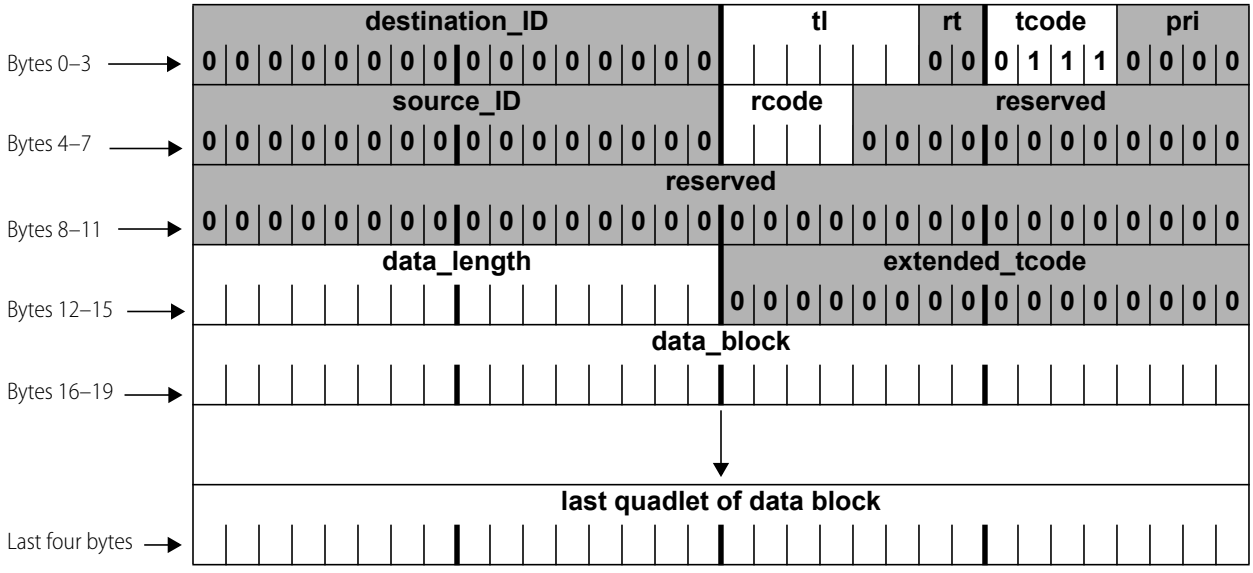


Read Block Request

Tcode = 5

Read Block Response

Tcode = 7



ERROR CODES

Response packets contain an *rcode* parameter, which shows whether the response is an ACK or a NAK. An *rcode* of 0 is an ACK; anything else is a NAK. If a NAK appears in the *rcode* parameter, check the Status area of the memory map (see page 92) to find out the reason for the NAK.

CAUTION: *If more than one client is communicating with the memory map (for example, your custom application and PAC Manager), you may read an error caused by a different client.*

The following table lists the error codes that may appear in the Status area of the memory map:

Code (Hex)	Meaning
0000	No error
E001	Undefined command
E002	Invalid channel type
E003	Invalid float
E004	Powerup Clear expected
E005	Invalid memory address or invalid data for the memory address
E006	Invalid command length
E007	Reserved

Code (Hex)	Meaning
E008	Busy
E009	Cannot erase flash
E00A	Cannot program flash
E00B	Downloaded image too small
E00C	Image CRC mismatch
E00D	Image length mismatch
E00E	Feature is not yet implemented
E00F	Communications watchdog timeout

A: Opto 22 Hardware Memory Map

INTRODUCTION

PR1
RIO
PAC-R
PAC-S
EB
SB
UIO
EIO
SIO
LCE
E1
E2
G4EB2

The tables on the following pages show all possible memory map locations for Opto 22 memory-mapped hardware devices. This memory map applies to all programming methods *except* EtherNet/IP, Modbus, and Optomux.

- For EtherNet/IP, see the EtherNet/IP for SNAP PAC Protocol Guide (form 1770).
- For Modbus, see the Modbus/TCP Protocol Guide (form 1678).
- For Optomux, see the Optomux Protocol Guide (form 1572).

The addresses available on your device are determined by the device type and model. Device types that support each section of the memory map are indicated at the beginning of the section (and sometimes for specific addresses).

NOTE: When using the memory map, ***ignore any addresses that don't apply to your device****; for example, ignore all analog addresses if you are using a digital-only I/O unit.*

Features for SNAP PAC I/O processors (brains, brain boards, and on-the-rack controllers) are detailed in Appendix A: Opto 22 Hardware Memory Map on page 165.

Features for *groov* EPIC processors and *groov* I/O modules are detailed in Appendix D: groov EPIC and groov RIO Features and Comparison Charts on page 169.

In This Chapter

NOTES ON COLUMNS

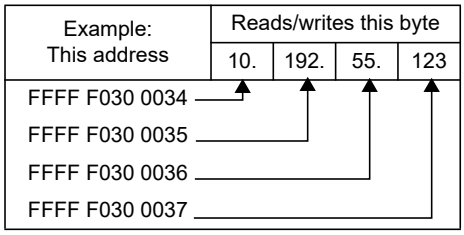
Starting Address—All memory map addresses are shown in hex notation. Note that addresses are shown with spaces for easier reading; when you use them, however, do not use spaces.

Length—The Length column shows the number of bytes in hex.

Type—Data type for the addresses is indicated as follows:

B	Boolean: Zero = false. Any non-zero value = true. (1-byte or 4-byte; see Length column for size)
BYTE	Byte (1-byte)
F	Float (4-byte)
I	Signed integer (1-byte, 2-byte, or 4-byte; see Length column for size)
UI	Unsigned integer (1-byte, 2-byte, or 4-byte; see Length column for size)
IP	IP address format (four 1-byte integers; see example following this table)
M	Mask (32-bit or 64-bit; see Length column for size)
S-ZT	String (null-terminated). The maximum length string allowed is one less than the total length, since the last character is always zero.
S-PL	String (prepended length)

IP address data type consists of four 1-byte integers. As shown in the example below, the lower-numbered address reads or writes the first byte:



BYTE ORDERING AND DATA ORDERING

All non-mask data for channels in bank and channel areas are arranged in low channel/low address order, as follows:

- Channel 0 at 0x....00

- Channel 1 at 0x....04
- Channel 2 at 0x....08

...and so forth.

All masks and multi-byte values (floats, integers, and so on) are in Big-Endian format, which means that the higher-ordered byte is in the lower-ordered address.

For more information and examples, see "Formatting and Interpreting Data" on page 58.

FOR EXPERIENCED OPTOMMP USERS

PR1
RIO
PAC-R
EB
SB

IMPORTANT: If you've used the memory map in the past, be aware that major changes occurred when firmware versions R8.0 and R8.1 were introduced for SNAP PAC controllers and brains. To accommodate new SNAP I/O modules with more than four channels, new expanded memory map areas were developed. While the older areas still work, we recommend using the expanded areas for new development, as they offer greater flexibility for the future.

NOTE: Expanded areas apply to groov I/O, groov RIO, SNAP PAC R-series, SNAP PAC EB, and SNAP PAC SB I/O units only. For SNAP Ultimate, Ethernet, Simple, E1, and E2 I/O units, continue to use the old areas.

If your custom application must accommodate devices with different firmware versions, you can try reading an address in the expanded area first. If you receive a response, use addresses in the expanded area. If there is no response, then use addresses in the old area.

Expanded areas and old areas are clearly marked in the memory map sections in this appendix. Here's a brief list of them:

Function	Expanded area		Old area		Notes
	Address	Page	Address	Page	
Analog and Digital Channel Configuration—Read/Write	F0100000	page 85	F0C00000	page 124	
Analog Channel Calc & Set	F01C0000	page 87	F0E00000	page 136	
Analog Channel Read & Clear	F01D4000	page 87	F0F80000	page 137	
Analog Channel Read	F0260000	page 88	F0A00000	page 123	
Analog Channel Write	F02A0000	page 89	F0B00000	page 123	
Digital Channel Read & Clear	F02E0000	page 90	F0F00000	page 136	
Digital Events - Expanded	F0D40000	page 127	F0D00000	page 127	Replaces Digital Events - Old. Expansion of Timers.
Scratch Pad - 64-bit Integers	F0DE0000	page 134	–	–	New Scratch Pad section
Analog EU or Digital Counter Packed Data Read	F1001000	page 139	–	–	Not a replacement
Digital Packed Data Read/Write	F1001800	page 139	–	–	Not a replacement

GENERAL NOTES

For OptoMMP devices, although it is possible to read or write up to 2,034 bytes at a time via TCP, performance will be significantly faster if you read about 1400 bytes or less at once.

Via UDP, the limit is 1,480 bytes.

Within these limits, you can read or write to large areas within the memory map using a block read or write. (Each area of the map is shown under a separate heading in the following pages.) If you are reading, just ignore any data in the reserved addresses between channels.

If you read or write beyond the last valid address in any area, however, you may receive an error.

Reading or writing in multiples of four bytes is recommended and is generally faster than accessing a number of bytes that is not a multiple of four.

CAUTION: *In certain areas, if you read or write less than a quadlet, the data will be useless. For example, reading two bytes of a float won't give complete data. Even more important, if you read only two bytes of a float in an area such as the Read and Clear area of the map, not only will the data you receive be useless, but also the information in the memory map will be erased (cleared).*

(EXPANDED) ANALOG & DIGITAL CHANNEL CONFIGURATION—READ/WRITE

PR1
RIO
PAC-R
EB
E1
E2
G4EB2

See page 16 for configuration information. For SNAP I/O units with firmware version R8.0 and newer, this area of the memory map replaces the F0C00000 area (page 124). To allow for future growth, this area has space for a total of 4096: an array of 64 channels per module on 64 modules. (*groov* I/O units and SNAP I/O units offer a maximum of 16 modules. A groov RIO I/O unit is one module, module 0.)

This area is stored to flash.

For E1 and E2 I/O units, remember to use only the first channel of each module. see "Referencing Module and Channel Positions on I/O Units" on page 9.

Only the first channel on the first module is shown in the table. Each successive channel starts on an even C0 hex boundary and follows the same pattern.

Starting Address	Length (Hex)	Type	Description
FFFF F010 0000	4	UI	Module 0, Channel 0 (0,0): Module Type (read only). Module type is the value reported by an analog, serial, or high-density digital module. Zero is returned for single or 4-channel digital modules, no module, or channels that don't exist (for example, the upper 62 channels on a two-channel analog module). For I/O module types, see the tables starting on page 127.
FFFF F010 0004	4	UI	0,0: Channel Type • Use 0x0000 0100 for single or 4-channel digital inputs. • Use 0x0000 0180 for single or 4-channel digital outputs. • For analog SNAP I/O types, see tables starting on page 21. For analog modules on an E2 I/O unit, see page 30.

Starting Address	Length (Hex)	Type	Description
FFFF F010 0008	4	UI	0,0: Channel Feature (unsigned integer) Digital feature values: • 0x0000 0001 for counter input (configures and starts the counter) • 0x0000 0002 for on-time totalizer input • 0x0000 0003 for period measurement (continuous) (Does not apply to *groov* I/O units or *groov* RIO modules.) • 0x0000 0004 for simple quadrature counter input • 0x0000 0005 for frequency measurement (continuous) (only for SNAP devices with SNAP firmware 8.0 and lower.) • 0x0000 0008 for frequency measurement (continuous) (for *groov* channels and SNAP devices with SNAP firmware R8.1a or higher) • 0x0000 0009 for on-pulse duration measurement (one-time) • 0x0000 000A for off-pulse duration measurement (one-time) • 0x0000 000B for period measurement (one-time) • 0x0000 000C for frequency measurement (one-time) • 0x0000 0012 for off-time totalizer input • 0x0000 0041 quadrature counter input with index. For quadrature counter information, see page 34. Analog feature values: none at present To disable channel features, use 0x0000 0000
FFFF F010 000C	4	F	0,0: Analog channel offset. Shows 0.0 unless you set an offset value. Brain uses the value you set or a default of 0.0.
FFFF F010 0010	4	F	0,0: Analog channel gain. Shows 0.0 unless you set a gain value. Brain uses the value you set or a default of 1.0.
FFFF F010 0014	4	F	0,0: Analog channel high scale (Engineering Units)
FFFF F010 0018	4	F	0,0: Analog channel low scale (EU)
FFFF F010 001C	4	–	0,0: Reserved
FFFF F010 0020	4	F	0,0: Average filter weight
FFFF F010 0024	4	F	0,0: Watchdog value. EU float for analog and digital (for digital, 0 = off; non-0 = on)
FFFF F010 0028	4	B	0,0: Enable watchdog. 0 = disable; non-0 = enable
FFFF F010 002C	4	–	0,0: Reserved
FFFF F010 0030	33	S-ZT	0,0: Channel name (50 characters plus a zero byte maximum)
FFFF F010 0063	1	–	0,0: Reserved
FFFF F010 0064	4	F	0,0 Steinhart-Hart Coefficient A
FFFF F010 0068	4	F	0,0 Steinhart-Hart Coefficient B
FFFF F010 006C	4	F	0,0 Steinhart-Hart Second Order Coefficient (use 0.0 if not specified)
FFFF F010 0070	4	F	0,0 Steinhart-Hart Coefficient C (use 0.0 if not specified)
FFFF F010 0074	4	UI	(Only for *groov* I/O units.) 0,0: Configuration bitmask. Bit 0 is the only recognized bit. Other bits are reserved for future use. Bit 0: Disable quality indication. Default value is 0 (meaning the quality indicator is enabled for this channel). • If this bit is set to 1, neither the module status LED nor the module quality bitmask at FFFF F100 2000 will indicate quality issues that occur on this channel. • If this bit is cleared, the module status LED will glow when there is quality issue for this channel.

Starting Address	Length (Hex)	Type	Description
FFFF F010 0078	10	S-ZT	(Only for *groov* I/O units and *groov* RIO modules.) 0,0: Channel Units null terminated string. The MMP server does not modify this area; the application must manage values in this area.
FFFF F010 0088	4	UI	(Only for *groov* I/O units.) 0,0: SMA (simple moving average) for analog filtering locally on the module. The module reserves only one byte for the value. A value of zero causes the module to use defaults. A higher value causes more samples to be averaged, with the net effect of less noise for higher values.
FFFF F010 008C	30	–	0,0 Reserved
FFFF F010 00B8	4	F	0,0: Analog channel lower clamp
FFFF F010 00BC	4	F	0,0: Analog channel upper clamp

Additional channels follow in order on even C0 hex boundaries.
Additional modules follow in order on even 3000 hex boundaries.

Last valid address for this area: FFFF F01B FFFF

(EXPANDED) ANALOG CHANNEL CALC & SET—READ/WRITE

PR1
RIO
PAC-R
EB
SB

See page 37 for more information on setting offset and gain. For SNAP I/O units with firmware version R8.0 and newer, this area of the memory map replaces the F0E00000 area (page 136). To allow for future growth, this area has space for 4096 channels, which is 64 channels per module on 64 modules. (*groov* I/O units and SNAP I/O units offer a maximum of 16 modules.)

See "IEEE Float Data" on page 61 for help in interpreting data.

Only the first two channels on the first module are shown in the table. Successive channels and modules follow the same pattern.

Starting Address	Length (Hex)	Type	Description
FFFF F01C 0000	4	F	Module 0, Channel 0 (0,0): Offset
FFFF F01C 0004	4	F	0,0: Gain
FFFF F01C 0008	4	F	0,1: Offset
FFFF F01C 000C	4	F	0,1: Gain

Additional channels follow in order.
Additional modules follow on even 200 hex boundaries.

Last valid address for this area: FFFF F01C 7FFF

(EXPANDED) ANALOG CHANNEL READ & CLEAR—READ/WRITE

PR1
RIO
PAC-R
EB
SB

See page 37 for more information on minimum and maximum values. For SNAP I/O units with firmware version R8.0 and newer, this area of the memory map replaces the F0F80000 area (page 137). To allow for future growth, this area has space for 4096 channels, which is 64 channels per module on 64 modules. (*groov* I/O units and SNAP I/O units offer a maximum of 16 modules.)

When you read data from this area, the data is returned and then cleared or reset. See "IEEE Float Data" on page 61 for help in interpreting data.

CAUTION: *If you read or write less than a quadlet in this area of the memory map, the returned data will be useless and the information will be erased (cleared).*

Only the first two channels on the first module are shown in the table. Successive channels and modules follow the same pattern.

Starting Address	Length (Hex)	Type	Description
FFFF F01D 4000	4	F	Module 0, Channel 0 (0,0): Minimum value
FFFF F01D 4004	4	F	0,0: Maximum value
FFFF F01D 4008	4	–	0,0: Reserved
FFFF F01D 400C	4	F	0,1: Minimum value
FFFF F01D 4010	4	F	0,1: Maximum value
FFFF F01D 4014	4	–	0,1: Reserved

Additional channels follow in order.
Additional modules follow in order on 300 hex boundaries.

Last valid address for this area: FFFF F01D FFFF

(EXPANDED) ANALOG CHANNEL READ—READ ONLY

PR1
RIO
PAC-R
EB
SB

For SNAP I/O units with firmware version R8.0 and newer, this area of the memory map replaces the F0A00000 area (page 123). To allow for future growth, this area has space for 4096 channels, which is 64 channels per module on 64 modules. (*groov* I/O units and SNAP I/O units offer a maximum of 16 modules.)

See "IEEE Float Data" on page 61 for help in interpreting data.

Only the first channel on the first module is shown in the table. Successive channels and modules follow the same pattern.

Starting Address	Length (Hex)	Type	Description
FFFF F026 0000	4	F	Module 0, Channel 0 (0,0): Analog channel value (Engineering Units)
FFFF F026 0004	4	F	0,0: Analog channel value (counts). (Does not apply to *groov* I/O units.)
FFFF F026 0008	4	F	0,0: Minimum value (EU)
FFFF F026 000C	4	F	0,0: Maximum value (EU)
FFFF F026 0010	12	–	Reserved.
FFFF F026 001C	4	UI	0,0: Reserved for load cell filter coefficient (Currently, always returns 0)
FFFF F026 0020	4	UI	0,0: (Does not apply to *groov* I/O units.) Reserved for analog-to-digital conversion count since last reading (Currently, always returns 0)
FFFF F026 0024	8	UI	0,0: Reserved for UI array. Used in SNAP modules to record the raw ADC counts (Currently, always returns {0,0})
FFFF F026 002C	4	UI	0,0: Quality indicator code. For a description and list of valid quality indicator codes, see "Quality Indicators" on page 171.
FFFF F026 0030	10	BYTE	0,0: Reserved

Additional channels follow in order on 40 hex boundaries.
Additional modules follow in order on 1000 hex boundaries.

Last valid address for this area: FFFF F029 FFFF

(EXPANDED) ANALOG CHANNEL WRITE—READ/WRITE

PR1
RIO
PAC-R
EB
SB

For SNAP I/O units with firmware version R8.0 and newer, this area of the memory map replaces the F0B00000 area (page 123). To allow for future growth, this area has space for 4096 channels, which is 64 channels per module on 64 modules. (*groov* I/O units and SNAP I/O units offer a maximum of 16 modules.)

See "IEEE Float Data" on page 61 for help in interpreting data.

Only the first channel on the first module is shown in the table. Successive channels and modules follow the same pattern.

Starting Address	Length (Hex)	Type	Description
FFFF F02A 0000	4	F	Module 0, Channel 0 (0,0): Analog channel value (Engineering Units)
FFFF F02A 0004	4	F	0,0: Analog channel value (counts)
FFFF F02A 0008	4	–	0,0: Reserved
FFFF F02A 000C	4	F	0,0: TPO period (units of time in seconds. Valid range: 0.00001 to 64.25 seconds.) (Not for E2s.)
FFFF F02A 0010	4	–	0,0: Reserved
FFFF F02A 0014	4	UI	0,0: Load cell fast settle level—For SNAP-AILC modules only. (Not for E2s.) Use with load cell filter weight (next address) to get filtered readings faster. Valid values: 0–32,767. 0 = disabled;
FFFF F02A 0018	4	UI	0,0: Load cell filter weight—For SNAP-AILC modules only. (Not for E2s.) Valid values: 0–255; default = 128. A larger value increases filtering. Use with F0B00014 to get the filtered reading faster. Note that 0, 1, or 255 value disables fast settle level (F0B00014). The second channel on the module is the filtered reading of the first channel.
FFFF F02A 001C	24	–	0,0: Reserved

Additional channels follow in order on 40 hex boundaries.
Additional modules follow in order on 1000 hex boundaries.

Last valid address for this area: FFFF F02D FFFF

(EXPANDED) DIGITAL CHANNEL READ—READ ONLY

PR1
RIO

Use this area to read *groov* I/O and *groov* RIO digital channels.
For SNAP high-density modules, see page 147. For other SNAP digital modules, see page 90.

Only the first channel on the first module is shown in the table. Successive channels and modules follow the same pattern.

Starting Address	Length (Hex)	Type	Description
FFFF F01E 0000	4	UI	Module 0, Channel 0 (0,0): Digital channel state
FFFF F01E 0004	4	UI	0,0: On latch
FFFF F01E 0008	4	UI	0,0: Off latch
FFFF F01E 000C	4	UI	0,0: Feature type. reports the selected feature type in (Expanded) Analog & Digital Channel Configuration—Read/Write address space FFFF F010 0008. Some feature types will auto clear when the measurement is complete
FFFF F01E 0010	4	UI/F	0,0: Feature value. Feature value is returned as an **integer** for edge counter, quadrature, on/off totalization, and pulses remaining. Feature value is returned as a **float** for period and frequency.

Starting Address	Length (Hex)	Type	Description
FFFF F01E 0014	4	UI	0,0: Quality indicator code. For a description and list of valid quality indicator codes, see "Quality Indicators" on page 171.
FFFF F01E 0018	4	UI	0,0: Counter active? 0 = no; non-0 = yes
FFFF F01E 001C	24	UI	0,0: Reserved

Additional channels follow in order on 40 hex boundaries.
Additional modules follow in order on 1000 hex boundaries.

Last valid address for this area: FFFF F021 FFFF

(EXPANDED) DIGITAL CHANNEL—READ/WRITE

PR1
RIO

Use this area to read and writer to *groov* digital channels. For SNAP high-density modules, see page 147. For other SNAP digital modules, see page 90.

Only the first channel on the first module is shown in the table. Successive channels and modules follow the same pattern.

Starting Address	Length (Hex)	Type	Description
FFFF F022 0000	4	UI	Module 0, Channel 0 (0,0): Digital channel state
FFFF F022 0004	4	UI	0,0: Start/resume channel counter feature. This value is automatically set to True when a *groov* counter feature type is set from the (Expanded) Analog & Digital Channel Configuration—Read/Write, offset 0x8. Writing a 0 (zero) has no effect. Writing a non-zero number starts (or resumes) counting edges.
FFFF F022 0008	4	UI	0,0: Stop channel counter feature. Writing a 0 (zero) has no effect. Writing a non-zero causes the feature value to stop reporting any edges seen—similar to a feature value freeze—until the counter is set active again by writing a non-zero value to FFFF F022 0004. Feature value is **not** cleared.
FFFF F022 000C	34	–	0,0: Reserved

Additional channels follow in order on 40 hex boundaries.
Additional modules follow in order on 1000 hex boundaries.

Last valid address for this area: FFFF F025 FFFF

(EXPANDED) DIGITAL CHANNEL READ & CLEAR—READ ONLY

PR1
RIO
PAC-R
EB
SB
G4EB2

For *groov* I/O, for *groov* RIO, and for SNAP I/O units with firmware version R8.0 and newer, this area of the memory map replaces the F0F00000 area (page 136). To allow for future growth, this area has space for 4096 channels, which is 64 channels per module on 64 modules. (*groov* I/O units and SNAP I/O units offer a maximum of 16 modules. *groov* RIO by definition is one module.)

When you read data from this area, the data is returned and then cleared. You can use this section for all *groov* and SNAP digital channels. For SNAP high-density modules, you can also use "High-Density Digital Read and Clear—Read/Write" on page 147.

Only the first channel on the first module is shown in the table. Successive channels and modules follow the same pattern.

Starting Address	Length (Hex)	Type	Description
FFFF F02E 0000	4	UI	Module 0, Channel 0 (0,0): Digital channel feature data.
FFFF F02E 0004	4	UI	0,0: On latch
FFFF F02E 0008	4	UI	0,0: Off latch
FFFF F02E 000C	4	–	0,0: Reserved

Additional channels follow in order on 18 hex boundaries.
Additional modules follow in order on 600 hex boundaries.

Last valid address for this area: FFFF F02F 7FFF

(EXPANDED) DIGITAL PACKED DATA—READ ONLY

PR1 RIO

(For *groov* I/O and *groov* RIO units only.) Like the Analog EU or Digital Counter Packed Data area (see page 139), this section is an efficient way to read *groov* channels with the fewest number of transactions.[1]

The data in this area is masked. The mask can hold the states of up to 32 channels, as illustrated below:

At address:	F1001900								→	F1001903							
These bit numbers:	7	6	5	4	3	2	1	0	→	7	6	5	4	3	2	1	0
Show data for these channels:	31	30	29	28	27	26	25	24	→	7	6	5	4	3	2	1	0

Only the first two modules are shown in the table. Successive modules follow the same pattern. Remember that a *groov* RIO unit is module 0.

Starting Address	Length (hex)	Type	Description
FFFF F100 1900	4	M	Module 0: Digital channel state mask (both digital input and digital output)
FFFF F100 1904	4	M	Module 0: Quality mask (set bit => bad quality, clear bit => good quality)
FFFF F100 1908	4	M	Module 0: On latch mask
FFFF F100 190C	4	M	Module 0: On latch mask
FFFF F100 1910	4	M	Module 1: Digital channel state mask (both digital and digital output)
FFFF F100 1914	4	M	Module 1: Quality mask (set bit => bad quality, clear bit => good quality)
FFFF F100 1918	4	M	Module 1: On latch mask
FFFF F100 191C	4	M	Module 1: On latch mask

Additional modules follow in order on 10 hex boundaries.

Last valid address for this area: FFFF F100 19FF

(EXPANDED) DIGITAL PACKED MUST ON/OFF (MOMO)—READ/WRITE

PR1 RIO

(For *groov* I/O and *groov* RIO units only.) This area provides an efficient way to turn *groov* channels off or on without having to know their current states and without affecting other channels. This means you can turn on a specific set of channels without first having to read all the channels' states to find out which ones are off and which are on.

The address space supports up to 64 modules.

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[1] Streaming is another method to efficiently get large amounts of data. For details, see "Streaming Data" on page 51, "Streaming Configuration—Read/Write" on page 119, and "Streaming—Read Only" on page 138.

The data in this area is masked. The mask can hold the states of up to 32 channels, as illustrated below:

At address:	F1001A00								→	F1001A03							
These bit numbers:	7	6	5	4	3	2	1	0	→	7	6	5	4	3	2	1	0
Show data for these channels:	31	30	29	28	27	26	25	24	→	7	6	5	4	3	2	1	0

To turn a channel on, set its State On bit to 1. If the channel is already on, it stays on. Clearing the bit (by sending a 0) has no effect. In this example, channels 0, 2, 3, and 8 are set to On.

Module 0: State **ON** mask address:	F1001A02								F1001A03							
Bit number:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Channel:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
On state:	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1

To turn a channel off, set its State Off bit to 1. If the channel is already off, it stays off. Clearing the bit (by sending a 0) has no effect. In this example, channels 4 and 5 are set to On.

Module 0: State **OFF** mask address:	F1001A04								F1001A05							
Bit number:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Channel:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Off state:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

When a channel's on bit and off bit are the same (either both 1s or both 0s), the channel is set to Off.

Only the first two modules are shown in the table. Successive modules follow the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F100 1A00	4	M	Module 0: State on mask
FFFF F100 1A04	4	M	Module 0: State off mask
FFFF F100 1A08	4	M	Module 1: State on mask
FFFF F100 1A0C	4	M	Module 1: State off mask

Additional modules follow in order on 8 hex boundaries.

Last valid address for this area: FFFF F100 1A7F

STATUS AREA READ—READ ONLY

PR1
RIO
PAC-R
PAC-S
EB
SB
UIO
EIO
SIO
LCE
E1
E2
G4EB2

This is the only area that can be read before sending a Powerup Clear message to the Opto 22 memory-mapped device. See "Sending Powerup Clear" on page 68 for more information.

Starting Address	Length (Hex)	Type	Description
FFFF F030 0000	4	UI	Memory Map revision number
FFFF F030 0004	4	UI	Powerup Clear flag (0 = OK; anything else means a Powerup Clear is needed)
FFFF F030 0008	4	UI	Busy flag (0 = not busy; anything else means the unit is busy and cannot process your request)
FFFF F030 000C	4	I	Last error code (see page 80)
FFFF F030 0010	2	UI	Transaction label for previous transaction (lower 6 bits)
FFFF F030 0012	2	UI	Source address of the unit that sent the request. Zero-filled unless you use the optional Source_ID parameter in the packet. See "Parameters" on page 76.

Starting Address	Length (Hex)	Type	Description
FFFF F030 0014	4	UI	Error address for last error (lower 32 bits of offset)
FFFF F030 0018	4	UI	Loader revision. 1st byte: major version number; 2nd byte: minor version number; 3rd byte: revision (0=A, 1=B, 2=R); 4th byte: letter (0=a, 1=b, 2=c, etc.) *Note: For groov, this value is always 0 (zero).*
FFFF F030 001C	4	IP	Firmware (kernel) revision. 1st byte: major version number; 2nd byte: minor version number; 3rd byte: revision (0=A, 1=B, 2=R); 4th byte: letter (0=a, 1=b, 2=c, etc.)
FFFF F030 0020	4	UI	Unit type of the device: 0x00000101 = GRV-EPIC-PR1 0x00000103 = GRV-R7-MM1001-10 0x0000004E = SNAP-PAC-R1-B 0x00000052 = OPTOEMU-SNR-DR2 0x00000056 = OPTOEMU-SNR-DR1 0x00000058 = G4EB2 0x0000005A = OPTOEMU-SNR-3V 0x0000005C = SNAP-PAC-SRA 0x00000062 = SNAP-PAC-SB2 0x00000064 = SNAP-PAC-SB1 0x00000066 = SNAP-PAC-R2-W 0x00000068 = SNAP-PAC-R1-W 0x0000006A = SNAP-PAC-S1-W 0x0000006C = SNAP-PAC-S2-W 0x00000070 = SNAP-PAC-EB2-W 0x00000072 = SNAP-PAC-EB1-W 0x00000074 = SNAP-PAC-EB2 0x00000076 = SNAP-PAC-EB1 0x00000078 = SNAP-PAC-R2 0x0000007A = SNAP-PAC-R1 0x0000007C = SNAP-PAC-S1 0x00000083 = SNAP-ENET-S64 0x0000008A = SNAP-UPN-ADS 0x0000008C = SNAP-UP1-M64 0x00000092 = SNAP-UP1-D64 0x00000093 = SNAP-UP1-ADS 0x00000094 = SNAP-WLAN-FH-ADS 0x00000097 = SNAP-ENET-D64 0x00000098 = SNAP-B3000-ENET or SNAP-ENET-RTC 0x000000E1 = E1 0x000000E2 = E2 0x00000193 = SNAP-LCE
FFFF F030 0024	1	UI	Hardware revision (Month)
FFFF F030 0025	1	UI	Hardware revision (Day)
FFFF F030 0026	2	UI	Hardware revision (Year)
FFFF F030 0028	4	UI	Number of bytes of installed RAM
FFFF F030 002C	2	–	Pad for alignment (Does not apply to SBs.)
FFFF F030 002E	6	UI	ENET1 MAC address. First three bytes of all Opto 22 Ethernet devices' MAC addresses are 00-A0-3D. (Does not apply to SBs.)
FFFF F030 0034	4	IP	ENET1 TCP/IP address (1.2.3.4 format: four 1-byte integers) (Not for SBs) (For ENET2, see FFFF F050.)
FFFF F030 0038	4	IP	ENET1 TCP/IP subnet mask (1.2.3.4 format: four 1-byte integers) (Not for SBs)
FFFF F030 003C	4	IP	ENET1 TCP/IP default gateway (1.2.3.4 format: four 1-byte integers) (Not for SBs)
FFFF F030 0040	4	IP	ENET1 DNS server address (1.2.3.4 format: four 1-byte integers) (Not for SBs)
FFFF F030 0044	4	–	Reserved
FFFF F030 0048	4	UI	Device sends BootP request (UIO, EIO, SIO, LCE) or DHCP request (E1, E2) when turned on: 0 = Only if device's IP address is 0.0.0.0. (Current IP address is static.) 1 = Whenever device is turned on. (Current IP address is dynamic.) (Does not apply to SBs.)
FFFF F030 004C	4	B	Degrees are in F or C (Valid only for I/O unit with analog capability) 0 = degrees C; non-0 = degrees F
FFFF F030 0050	4	–	Reserved
FFFF F030 0054	4	UI	Watchdog time in milliseconds (unsigned integer). 0 means watchdog is disabled.

Starting Address	Length (Hex)	Type	Description
FFFF F030 0058	4	UI	TCP/IP minimum Response Timeout (RTO) in milliseconds. TCP/IP calculates the RTO based on past network response times. The default is a minimum 3000 msec between retries. (Does not apply to E1s, E2s, SBs.)
FFFF F030 005C	4	UI	Digital scan counter. Counts the number of scans of these digital modules; can be used for benchmarking. (Does not apply to *groov* Simple modules or E1s.)
FFFF F030 0060	4	UI	Analog and digital scan counter. Counts the number of scans of analog and HDD modules; can be used for benchmarking. (Does not apply to *groov* Simple modules.)
FFFF F030 0064	4	UI	Initial RTO. (Does not apply to E1s, E2s, SBs.)
FFFF F030 0068	4	UI	TCP number of retries. (Does not apply to E1s, E2s, SBs.)
FFFF F030 006C	4	UI	TCP idle session timeout. (Does not apply to E1s, E2s, SBs.)
FFFF F030 0070	4	UI	Ethernet errors: late collisions. This and the next two sets of addresses indicate problems on the Ethernet network, often due to length of the segment or number of devices. Late collisions are not normal. Normally two Ethernet hosts trying to talk at once collide early in the packet and both back off, or the second host waits. (Does not apply to E1s, E2s, SBs.)
FFFF F030 0074	4	UI	Ethernet errors: excessive collisions. Indicate that all the backup attempts to communicate have been exhausted. (Does not apply to E1s, E2s, SBs.)
FFFF F030 0078	4	UI	Ethernet errors: other. (Does not apply to E1s, E2s, SBs.)
FFFF F030 007C	4	M	“Smart” modules present. Bitmask showing the presence of analog, serial, high-density digital, and PID modules. Present = 1; not present = 0. Use as a troubleshooting tool to make sure modules are online. Note that all *groov* I/O and *groov* RIO modules are “smart.” (Does not apply to E1s, E2s, G4EB2s.)
FFFF F030 0080	20	S-ZT	Device’s part number (string)
FFFF F030 00A0	10	S-ZT	Firmware version date
FFFF F030 00B0	10	S-ZT	Firmware version time
FFFF F030 0100	4	UI	ARCNET reconfigs detected. Indicates that a “smart” module (analog, serial, high-density digital) has been added, removed, or reset. This and the other addresses starting with ARCNET refer to the ARCNET bus used on the rack for communication between the I/O processor and I/O modules. (Does not apply to E1s, E2s, G4EB2s.)
FFFF F030 0104	4	UI	ARCNET reconfigs initiated by I/O unit. Error on the rack’s ARCNET bus. (Does not apply to E1s, E2s, G4EB2s.) Not a concern unless it happens frequently. If there are no analog, serial, high-density digital, or PID modules on the rack, ignore it. If there is at least one of these modules on the rack, make sure the rack has adequate voltage.
FFFF F030 0108	4	UI	Number of times the device closed the session because it was idle. (Does not apply to E1s, E2s, SBs.)
FFFF F030 010C	4	UI	Milliseconds since powerup. Value rolls over after 4,294,967,295 ms, which is equal to 49.71 days. For longer periods of time, use address F030 0160 (in seconds) or F030 0228 (64-bit field, in milliseconds). (Does not apply to E1s or E2s.)
FFFF F030 0110	4	UI	Ethernet MAC resets since powerup. Caused by electrical noise. (Does not apply to E1s, E2s, SBs.)
FFFF F030 0114	4	UI	Digital output channel resets since powerup. Caused by electrical noise. (Does not apply to *groov* channels, E1s, or E2s.)
FFFF F030 0118	4	UI	Digital interrupt failures since powerup. Digital counter may have missed counts. (Does not apply to *groov* channels, E1s, or E2s.)

Starting Address	Length (Hex)	Type	Description
FFFF F030 011C	4	UI	Total number of PID loops available on this I/O unit (96 for SNAP PAC R-series, 32 for UIO, 16 for EIO, none for other I/O units).
FFFF F030 0120	4	UI	ARCNET transmit attempts since powerup. (Not on E1s, E2s, G4EB2s.)
FFFF F030 0124	4	UI	ARCNET other (node not found, etc.). (Not on E1s, E2s, G4EB2s.)
FFFF F030 0128	4	UI	ARCNET ACKs. (Not on E1s, E2s, G4EB2s.)
FFFF F030 012C	4	UI	ARCNET delay between transmit attempt and ACK for most recent attempt. (Not on E1s, E2s, G4EB2s.)
FFFF F030 0130	4	UI	ARCNET timeout value (msec.). (Not on E1s, E2s, G4EB2s.)
FFFF F030 0134	4	UI	ARCNET timeouts. (Not on E1s, E2s, G4EB2s.)
FFFF F030 0138	4	UI	ARCNET receive interrupts. (Not on E1s, E2s, G4EB2s.)
FFFF F030 013C	4	–	Reserved
FFFF F030 0140	4	F	Milliseconds per analog/HDD scan. Value of -1 means scanner is not running.
FFFF F030 0144	4	F	Milliseconds per digital (4-ch) scan. Value of -1 means scanner is not running. (Does not apply to *groov* channels.)
FFFF F030 0148	4	UI	Number of single or 4-channel digital modules supported (0, 8, or 16). Useful for SNAP-PAC-R1s; R1s with serial numbers below 600,000 support only 8 (in the first 8 rack positions); newer modules support 16. Added in SNAP firmware R8.1; older SNAP firmware doesn't include this address.
FFFF F030 014C	4	UI	(SB brains only) Brain's unique serial number (SB brains do not have a MAC address).
FFFF F030 0150	4	UI	(SB brains only) Multidrop address
FFFF F030 0154	4	UI	(SB brains only) Baud rate.
FFFF F030 0158	4	UI	(SB brains only) Number of framing errors during serial transmission (no stop bit detected). Should be zero under normal operation; if it is anything other than zero, the baud rate may be incorrect or there may be noise on the serial bus.
FFFF F030 015C	4	UI	(SB brains only) Number of FIFO overrun errors. Should be zero under normal operation. Contact Opto 22 Product Support if any other number appears in this field.
FFFF F030 0160	4	UI	Elapsed time since powerup (in seconds). Use instead of F030 010C for longer periods of time. Value rolls over after 4,294,967,295 seconds, which is equal to 49,710 days. (Does not apply to E1s or E2s.)
FFFF F030 0164	C4	–	Reserved
FFFF F030 0228	8	UI	Milliseconds since powerup. Use instead of F030 010C for longer periods of time in milliseconds. Value rolls over after 584,542,046 years. (Does not apply to E1s or E2s.)
FFFF F030 0230	4	UI	(PAC-R and PAC-S only, SNAP firmware R8.4a and higher. Does not apply to PR1 or RIO.) Current boot device: 0 = Flash memory; 1 = microSD card.
FFFF F030 0234	14	–	Reserved
FFFF F030 0248	4	I	Result of some Status Area Write commands (F0380000 on page 101). Results apply only to commands 03, 04, 0D, 0E, 0F, and 10. 0 = Operation was successful. -109 = microSD card is read only. -110 = microSD card is not inserted. -111 = Controller doesn't support microSD cards.

Starting Address	Length (Hex)	Type	Description
FFFF F030 024C	4	UI	Firmware revision. 1st byte: major version number; 2nd byte: minor version number; 3rd byte: revision (0=A, 1=B, 2=R); 4th byte: letter (0=a, 1=b, 2=c, and so forth)

Last valid address for this area: FFFF F030 0250

MODULE BUILD DATA–READ ONLY

PR1
RIO

This area provides information about the *groov* modules on the I/O unit. 128 bytes are available for each module.

Only the first module is shown in the table. Successive modules follow the same pattern. Remember that *groov* RIO is module 0.

Starting Address	Length (Hex)	Type	Description
FFFF F811 0000	4	UI	0,0: Module 0. Module type. For a list of module type codes, see page 16.
FFFF F811 0004	4	UI	Reserved
FFFF F811 0008	4	UI	Firmware mode. For kernel mode, returns 0x6B or `k`. For loader mode, returns 0x6C or `l`.
FFFF F811 000C	4	UI	Manufacturer's serial number.
FFFF F811 0010	4	–	Hardware revision • 1st byte: Month • 2nd byte: Day • 16-bit word: Year
FFFF F811 0014	28	–	Loader revision • 32-bit double word: Program number • Byte: Major version number • Byte: Minor version number • Byte: Build type. 0 = Alpha, 1 = Beta, 2 = Release • Byte: Maintenance letter. 0 = a, 1 = b, and so forth • 10-byte string: Version Date MM/DD/YYYY • 8-byte string: Version Time HH:MM:SS (24-hour)
FFFF F811 003C	28	–	Firmware (kernel) revision • 32-bit double word: Program number • Byte: Major version number • Byte: Minor version number • Byte: Build type. 0 = Alpha, 1 = Beta, 2 = Release • Byte: Maintenance letter. 0 = a, 1 = b, and so forth • 10-byte string: Version Date MM/DD/YYYY • 8-byte string: Version Time HH:MM:SS (24-hour)
FFFF F811 0064	4	–	Reserved

Additional modules follow in order on 80 hex boundaries.

Last valid address for this area: FFFF F811 07FF

QUALITY OF DATA–READ ONLY

PR1
RIO

This area provides information about the quality indicators in *groov* I/O and *groov* RIO modules. Use this address space to find out which *groov* modules and channels are reporting a quality indicator code. A code of 0 means data quality is good; no exceptions have occurred. For a list of valid quality indicator codes, see "Quality Indicators" on page 171.

Bitmask example:

At address:	F1002000								→	F1002007							
These bit numbers:	7	6	5	4	3	2	1	0	→	7	6	5	4	3	2	1	0
Show data for these modules:	63	62	61	60	59	58	57	56	→	7	6	5	4	3	2	1	0

To prevent channels from indicating quality, see address space FFFF F010 0074, "(Expanded) Analog & Digital Channel Configuration—Read/Write" on page 85.

Only the first module and its first four channels are shown in the table. Successive modules and channels follow the same pattern.

Starting Address	Length (Hex)	Type	Description
FFFF F100 2000	8	M	Quality indicators present. Bitmask shows which modules have at least one channel reporting a quality indicator code. This area supports up to 64 modules. A bit in this mask will clear only when no channels in the module have a quality indicator. If a channel has a value of 1 in address space FFFF F010 0074, its quality indicators are not counted in toward the module's total number of indicators present. (See "(Expanded) Analog & Digital Channel Configuration—Read/Write" on page 85.)
FFFF F100 2008	78	–	Reserved
FFFF F100 2080	4	UI	(0,0) Quality indicator code for Module 0, Channel 0. For a description and list of valid quality indicator codes, see "Quality Indicators" on page 171.
FFFF F100 2084	4	UI	(0,1): Quality indicator code for Module 0, Channel 1
FFFF F100 2088	4	UI	(0,2): Quality indicator code for Module 0, Channel 2
FFFF F100 208C	4	UI	(0,3): Quality indicator code for Module 0, Channel 3

Additional channels follow in order on 4 hex boundaries.
Additional modules follow in order on 100 hex boundaries.

Last valid address for this area: FFFF F100 607F

COMMUNICATIONS PORT CONFIGURATION—READ/WRITE

PAC-R
PAC-S
UIO
LCE

Use this area of the memory map to configure the serial ports on a SNAP PAC, SNAP-LCE, or SNAP Ultimate controller. (Does not apply to *groov* I/O units.) See the device's user guide for numbers of ports and port locations. See the *PAC Manager User's Guide* for configuration information.

Starting Address	Length (hex)	Type	Description
FFFF F031 0400	4	UI	Port 0: Control function for serial port. Default is 1. LCE, PAC-R, or UIO must be rebooted if value is changed; PAC-S does not have to be rebooted. See device's user guide for port locations and details. 0 = None (used with PAC Control to connect directly to serial I/O units or devices, depending on controller capabilities) 1 = PPP (for modem use). Only one port should be configured for PPP. 2 = Nokia - M2M (not valid for PAC-S1)

Starting Address	Length (hex)	Type	Description
FFFF F031 0404	4	UI	Port 0: Enable logging. 0 = Disabled; 1 = Enabled. Default is 0. If control function is set to None (0), received characters are only logged if they've been retrieved by the PAC Control strategy. All data received and transmitted is logged to a binary file named Comm<port number>.log, stored in the device's file system. Each byte of data is stored as two bytes: the first is data direction (capital letter `I` = received data; capital letter `O` = transmitted data); the second is the data itself. Maximum size of the log file is 16,384 bytes; beyond this limit, new data replaces the oldest data. A null character (ASCII code 0) with no data direction prepended follows the most recent data logged. This value takes effect immediately. If you use this port to retrieve the log file from the file system, always set this value to 0 before retrieval, or the log will be filled with data generated by the file transfer.
FFFF F031 0408	4	UI	Port 1: Control function for serial port. Default is 0. Valid value for PAC-S1 is 0. See device's user guide for port locations and details. 0 = None (used with PAC Control to connect directly to serial I/O units or devices, depending on controller capabilities) 1 = PPP (for modem use). Only one port should be configured for PPP. 2 = Nokia - M2M.
FFFF F031 040C	4	UI	Port 1: Enable logging. 0 = Disabled; 1 = Enabled. Default is 0. Same as port 0 logging.
FFFF F031 0410	4	UI	Port 1: Control function for serial port. Default is 0. Valid value for PAC-S1 is 0. See device's user guide for port locations and details. 0 = None (used with PAC Control to connect directly to serial I/O units or devices, depending on controller capabilities) 1 = PPP (for modem use). Only one port should be configured for PPP. 2 = Nokia - M2M.
FFFF F031 0414	4	UI	Port 1: Control function for serial port. Default is 0. Valid value for PAC-S1 is 0. See device's user guide for port locations and details. 0 = None (used with PAC Control to connect directly to serial I/O units or devices, depending on controller capabilities) 1 = PPP (for modem use). Only one port should be configured for PPP. 2 = Nokia - M2M.
FFFF F031 0418		–	Reserved
FFFF F031 0800	4	UI	(PAC-S & PAC-R only) Port 0: Read only. Detects a failed link by checking CD signal. 0 = deasserted (failed); 1 = asserted.
FFFF F031 0804	4	UI	(PAC-S & PAC-R only) Port 0: Read/write. DTR; hangs up the modem (modem must be configured with &D2). 0 = deassert; 1 = assert.
FFFF F031 0808	4	UI	(PAC-S & PAC-R only) Port 0: Read only. DSR. 0 = deasserted; 1 = asserted
FFFF F031 080C	4	UI	(PAC-S & PAC-R only) Port 0: Read/write. RTS. 0 = deassert; 1 = assert
FFFF F031 0810	4	UI	(PAC-S & PAC-R only) Port 0: Read only. CTS. 0 = deasserted; 1 = asserted
FFFF F031 0814	4	UI	(PAC-S & PAC-R only) Port 0: Read only. RI. 0 = deasserted; 1 = asserted
FFFF F031 0818	10	–	Reserved
FFFF F031 082C	4	UI	(PAC-S & PAC-R only) Port 1: Read/write. RTS. 0 = deassert; 1 = assert
FFFF F031 0830	4	UI	(PAC-S & PAC-R only) Port 1: Read only. CTS. 0 = deasserted; 1 = asserted
FFFF F031 0834	14	–	Reserved
FFFF F031 084C	4	UI	(PAC-S only) Port 2: Read/write. RTS. 0 = deassert; 1 = assert

<table>
<tr><th>Starting Address</th><th>Length (hex)</th><th>Type</th><th>Description</th></tr>
<tr><td>FFFF F031 0850</td><td>–</td><td>–</td><td>Reserved</td></tr>
<tr><td>FFFF F031 0C00</td><td>4</td><td>UI</td><td>PAC-R and PAC-S only (each has one programmable LED, the PPP LED). Indicates what controls the PPP LED to indicate the current PPP state. Can be stored to flash.
0 = None
1 = Programmable LED state address (F0310E00) controls the LED.
2 = (Default) PPP service controls the LED; state is indicated as follows:
<table>
<tr><th>LED action</th><th>Indicates state</th></tr>
<tr><td>Off</td><td>Idle (0) or Disabled (9)</td></tr>
<tr><td>Slow blink green</td><td>Outgoing connecting (1) or
Incoming connecting (5)</td></tr>
<tr><td>Solid green</td><td>Outgoing connected (2) or
Incoming connected (6)</td></tr>
<tr><td>Slow blink orange</td><td>Outgoing disconnecting (3) or
Incoming disconnecting (7)</td></tr>
<tr><td>Solid orange</td><td>Listen (4)</td></tr>
<tr><td>Slow blink red</td><td>Shutting down (8)</td></tr>
</table></td></tr>
<tr><td>FFFF F031 0C04</td><td></td><td>–</td><td>Reserved</td></tr>
<tr><td>FFFF F031 0E00</td><td>4</td><td>UI</td><td>PAC-R and PAC-S only. State for programmable PPP LED.
0 = Off
1 = Green
2 = Red
3 = Orange (green and red at the same time)</td></tr>
<tr><td>FFFF F031 0E04</td><td>–</td><td>–</td><td>Reserved</td></tr>
<tr><td>FFFF F031 1100</td><td>4</td><td>UI</td><td>(PAC-S2 only) Port 0 Mode
<table>
<tr><td>0</td><td>None (all signals set to high impedance inputs)</td></tr>
<tr><td>232</td><td>RS-232 (default)</td></tr>
<tr><td>24850</td><td>2-wire RS-485, no bias, no termination</td></tr>
<tr><td>24852</td><td>2-wire RS-485, bias, no termination</td></tr>
<tr><td>24851</td><td>2-wire RS-485, no bias, termination</td></tr>
<tr><td>24853</td><td>2-wire RS-485, bias, termination</td></tr>
<tr><td>44850</td><td>4-wire RS-485, no bias, no termination</td></tr>
<tr><td>44852</td><td>4-wire RS-485, bias, no termination</td></tr>
<tr><td>44851</td><td>4-wire RS-485, no bias, termination</td></tr>
<tr><td>44853</td><td>4-wire RS-485, bias, termination</td></tr>
</table></td></tr>
<tr><td>FFFF F031 1104</td><td>4</td><td>UI</td><td>(PAC-S2 only) Port 1 Mode, same values as above</td></tr>
<tr><td>FFFF F031 1108</td><td>4</td><td>UI</td><td>(PAC-S2 only) Port 2 Mode, same as above except default is 24853</td></tr>
<tr><td>FFFF F031 110C</td><td>4</td><td>UI</td><td>(PAC-S2 only) Port 3 Mode, same as above except default is 24853</td></tr>
</table>

Last valid address for this area: FFFF F031 110F

SERIAL PASS-THROUGH—READ/WRITE

Use this area of the memory map only to talk to a SNAP PAC SB (serial) brain through an S-series or R-series controller's serial port (called *serial pass-through)*. This area contains a configuration section and a data section. Configure the port first; then write to the data section to send a memory map packet; finally, read the data section to read the response.

Configuration—For each serial port, write all fields in the configuration area at once, in one memory map packet. Once the port has been enabled, you can change only the Timeout field by writing to it individually.

Data—Write to send an OptoMMP packet out the serial port. Read to see the response to the packet you sent. You will not get an ACK back until the response is ready to be read.

Starting Address	Length (Hex)	Type	Description
Configuration Section (write all in one MemMap packet)			
FFFF F032 9000	4	UI	Port 0: enable serial pass-through (0 = disabled; non-zero = enabled)
FFFF F032 9004	4	UI	Port 0: data rate (bps)
FFFF F032 9008	4	UI	Port 0: number of data bits
FFFF F032 900C	4	UI	Port 0: parity: 0x4E None 0x45 Even 0x4F Odd 0x4D Mark 0x53 Space 0x44 9th bit multidrop
FFFF F032 9010	4	UI	Port 0: number of stop bits
FFFF F032 9014	4	UI	Port 0: 2-wire or 4-wire (0x48 = 2-wire; 0x46 = 4-wire)
FFFF F032 9018	4	UI	Port 0: timeout in ms. Number of ms to wait for a response. This address can be written to individually after initial configuration.
FFFF F032 A000	–	–	Port 1 configuration (same pattern as port 0, above)
FFFF F032 B000	–	–	Port 2, same pattern
FFFF F032 C000	–	–	Port 3, same pattern
FFFF F032 D000	–	–	Port 4, same pattern
FFFF F032 E000	–	–	Port 5, same pattern
Data Section (write to transmit; read to see response)			
FFFF F032 9100	4	UI	Port 0: Write = 8-bit multidrop address of the serial brain Read = 16-bit length of the response field (F0329104)
FFFF F032 9104	4	UI	Port 0: Write = 8-bit packet type identifier (OptoMMP packet = 0x02) Read = OptoMMP response.
FFFF F032 9108	4	UI	Port 0 (Write only): 16-bit length of the packet (F032910C)
FFFF F032 910C	4	UI	Port 0 (Write only): packet containing memory map command
FFFF F032 A100	–	–	Port 1 configuration (same pattern as port 0, above)
FFFF F032 B100	–	–	Port 2, same pattern
FFFF F032 C100	–	–	Port 3, same pattern
FFFF F032 D100	–	–	Port 4, same pattern
FFFF F032 E100	–	–	Port 5, same pattern

Last valid address for this area: FFFF F032 EFFF

DATE AND TIME CONFIGURATION—READ/WRITE

PAC-R
EB
SB
UIO
EIO
G4EB2

Use this area of the memory map to view or change the date and time on SNAP PAC R-series, SNAP PAC EB or SB, SNAP Ultimate, or SNAP-ENET-RTC, which contain a real-time clock. (Does not apply to *groov* I/O units.) On other devices you cannot set the date and time; this area shows the elapsed time since the device was last turned on.

Starting Address	Length (hex)	Type	Description
FFFF F035 0000	16	S-ZT	Set date and time. Format: YYYY-MM-DD HH:MM:SS.00

Last valid address for this area: FFFF F035 0023

STATUS AREA WRITE—READ/WRITE

PR1
RIO
PAC-R
PAC-S
EB
SB
UIO
EIO
SIO
LCE
E1
E2
G4EB2

This area is read/write, but you would normally write to it. The area as a whole applies to all memory-mapped devices, but some addresses or codes apply to some devices and not others (see Appendix C: SNAP Features Comparison Chart and Appendix D: groov EPIC and groov RIO Features and Comparison Charts).

When you write to this area, you must write all four bytes, or you'll receive an "invalid memory address" error. You can write to this area using either a quadlet or a block write.

Starting Address	Length (hex)	Type	Description
FFFF F038 0000	4	UI	Operation code (Some results returned in F0300248, page 95.) 0x000000**01** – Send Powerup Clear 0x000000**02** – Reset to defaults (clears I/O configuration and erases it from flash; also clears scratch pad areas, PIDs, and TPOs.) **CAUTION:** See "Details on Operation Codes in Address F0380000" on page 103. 0x000000**03** – Stores scratch pad areas to flash. (For *groov* I/O units only, all remaining configuration areas are autosaved to flash.) **CAUTION:** See details on page 103. 0x000000**04** – Erase all configuration from flash memory and microSD card. **CAUTION:** See details on page 103. The following address spaces do not apply to *groov* I/O or RIO units: 0x000000**05** – Reset hardware, which is just like cycling power to the device. If channel configuration information has not been stored to flash or flash has been cleared (op code 04), channels are reset to defaults. After a hardware reset, the device waits for a Powerup Clear before communicating. 0x000000**06** – Clear "Digital Events - Old" configuration (for expanded digital events in SNAP firmware R8.1 or higher, use 0x0000000A below). 0x000000**07** – Clear Alarms configuration. 0x000000**08** – Clear PPP configuration. (Not on EB, SB, G4EB2.) 0x000000**09** – Clear Email configuration. (Does not apply to SB.) 0x000000**0A** – Clear "Digital Events - Expanded" configuration (For SNAP firmware R8.0 and lower, clears Timers configuration). 0x000000**0B** – Clear PID loops configuration (analog devices only). 0x000000**0C** – Clear data log. 0x000000**0D** – Save configuration and IP address to microSD card. See details on page 103. 0x000000**0E** – Erase configuration and IP address from microSD card. See details on page 103. 0x000000**0F** – Erase firmware from microSD card. See page 103. 0x000000**10** – Erase strategy from microSD card. See page 103. 0x**87654321** – Boot to loader. (UIO, EIO, SIO, and LCE only)

Starting Address	Length (hex)	Type	Description
FFFF F038 0004	4	UI	Set device to send BootP or DHCP request when turned on. 0 (default for all except E1 & E2) = Send BootP or DHCP request only if device's IP address is 0.0.0.0. Current IP address is saved to flash memory and becomes a static IP address. 1 (default for E1 & E2) = Always send BootP or DHCP request when device is turned on. IP address is dynamic (temporary). (Does not apply to SBs.)
FFFF F038 0008	4	B	Set degrees in F or C. 0 (default) = degrees C; non-0 = degrees F
FFFF F038 000C	4	–	Reserved
FFFF F038 0010	4	UI	Set watchdog time in milliseconds (unsigned integer). 0 disables watchdog.
FFFF F038 0014	4	UI	Set TCP/IP minimum Response Timeout (RTO) in milliseconds. (Does not apply to E1s, E2s, or SBs.) For SNAP PAC R-series, SNAP PAC EB, SNAP Ultimate, and SNAP Simple I/O units, the default is a minimum 100 msec between retries. For SNAP Ethernet I/O units, the default is a minimum 3000 msec between retries. For a high-speed application such as motion control, you can write a lower minimum RTO to this address.
FFFF F038 0018	4	UI	Set TCP/IP initial RTO. (Does not apply to E1s, E2s, or SBs.)
FFFF F038 001C	4	UI	Set TCP/IP number of retries. (Does not apply to E1s, E2s, or SBs.)
FFFF F038 0020	4	UI	TCP idle session timeout in milliseconds. 0 = disable. (Does not apply to E1s, E2s, or SBs.)
FFFF F038 0024	4	UI	Wireless configuration: mode (Does not apply to SBs.)
FFFF F038 0028	4	UI	Wireless configuration: ESS identification (Does not apply to SBs.)
FFFF F038 002C	20	–	Reserved
FFFF F038 004C	4	UI	(Does not apply to *groov* I/O or *groov* RIO units.) Set maximum digital scan interval for single or 4-channel digital modules, in milliseconds. (This value is ignored in SNAP firmware R8.1 and higher; use F038 0294 instead. Not for E1s or E2s.) Default = 1000 (1 sec). Setting the value to -1 shuts down the scanner until power is cycled.
FFFF F038 0050	4	UI	(Does not apply to *groov* I/O or *groov* RIO units.) Set maximum analog and high-density digital scan interval (msec). (Not for E1s, E2s, G4EB2s.) Setting the value to -1 shuts down the analog/HDD scanner until power is cycled. As of SNAP firmware version R8.1, analog modules with more than 4 channels are scanned no faster than every 30 ms, and analog modules with four or fewer channels are scanned no faster than every 6 ms, in order to maintain synchronization with the module.
FFFF F038 0054	4	M	(Does not apply to *groov* I/O or *groov* RIO units.) Scanner Flags. Used to maximize speed under special circumstances. Binary mask: 0 = Off; 1 = On. Use one or a combination of the following bits. All except the first one require that the I/O unit be restarted. 0x01 = Handle alarms in digital (single/4-ch) scanner rather than analog/HDD scanner 0x02 = Stop analog/HDD/ serial module scanner 0x04 = Stop digital (single/4-ch) scanner 0x08 = Stop PAC Control engine (SNAP PAC R-series and UIO only) (Example: 0100 = Stop digital (4-ch) scanner flag is on; all other scanner flags are off. This means that alarms are handled in the analog/HDD scanner, the analog/HDD scanner is running, the digital (4-ch) scanner is stopped, and the PAC Control engine is running.)
FFFF F038 0058	4	M	(Does not apply to groov I/O or *groov* RIO units.) ON mask for scanner flags (see F038 0054). 1 = On; 0 = No change

Starting Address	Length (hex)	Type	Description
FFFF F038 005C	4	M	(Does not apply to groov I/O or *groov* RIO units.) OFF mask for scanner flags (see F038 0054). 1 = On; 0 = No change
FFFF F038 0060	F4	–	Reserved
FFFF F038 0154	40	S-ZT	Host Name (E1 and E2 only). Used only if the unit has a dynamic IP address assigned by the network.
FFFF F038 0194	100	S-ZT	Domain Name (E1 and E2 only).
FFFF F038 0294	4	UI	(Does not apply to groov I/O or *groov* RIO units.) Sets the digital scan interval. Most reading and writing to 4-ch digital I/O happens asynchronously. However, the following features are updated once per digital scan: digital events - old, digital events -enhanced (formerly Timers), frequency and period measurement, data logging, and alarms if digitally scanned (see F038 0054, Scanner Flags).
FFFF F038 0298	4	F	Value shown for modules that return a 16-bit value to the brain, when actual value is out of range. Default is –32,768
FFFF F038 02B0	4	F	Value shown for modules that return a 32-bit value to the brain, when actual value is out of range. Default is –2,147,483,648

Last valid address for this area: FFFF F038 02B3

Details on Operation Codes in Address F0380000

NOTE: Many of these op codes affect a microSD card, if the device has one. See the device's user's guide for important information before using the card.

Results for op codes 03, 04, 0D, 0E, 0F, 10, and 11 are returned in F0300248 (see page 95).

0x02—Resets device to defaults (equivalent to an 04 op code followed by an 05). Requires a Powerup Clear after resetting.
CAUTION: If you have SNAP firmware 9.0 or newer and a microSD card is present, this code also erases any firmware, strategy, IP address, and configuration data from the card. This code does not erase other data files on the microSD card.

If you have older SNAP firmware versions, these files on the microSD card are not erased.

0x03—Stores all configuration data to flash memory, so it is restored when the device is turned on.
CAUTION: If you have SNAP firmware 9.0 or newer and a microSD card is present, and if the card already has IP address and configuration data stored on it (see op code 0D), code 03 also overwrites the configuration data and IP address on the card with the new configuration.
Exception: On a controller using Secure Strategy Distribution (SSD), configuration data is stored to flash but not to the microSD card.
Other data files on the microSD card are not affected.
If you have older SNAP firmware versions, nothing is saved to the microSD card.

0x04—Erases all configuration data from flash memory and microSD card. Details:

- Erases all IP address and configuration data from the microSD card, if one is present and has IP and configuration data stored on it (see op code 0D). Firmware and strategy files on the card are not erased. Other data files are not erased.
- Clears error information in the status area (F030000C, etc.: error code, transaction label, source address, error address).
- Clears gains and offsets, latches, min/max data, and counters. Deactivates counters.
- Turns off digital outputs.
- Sets analog outputs to zero scale (0 counts).

0x0D—Requires SNAP firmware 9.0 or newer. Applies only to devices with a microSD card slot and a card in place. Stores the controller's IP address and configuration data on the microSD card.
Exception: Data is not stored to a card in a controller using Secure Strategy Distribution (SSD).

0x0E—Requires SNAP firmware 9.0 or newer. Applies only to devices with a microSD card slot and a card in place. Erases IP address and configuration data from the microSD card. Does not erase any other files.

0x0F—Requires SNAP firmware 9.0 or newer. Applies only to devices with a microSD card slot and a card in place. Erases firmware from the microSD card in the boot directory and in all locations mentioned in the firmware command file. Also erases firmware command and response files from the card. Does not erase IP address, configuration, strategy, or data files from the card.

0x10—Requires SNAP firmware 9.0 or newer. Applies only to devices with a microSD card slot and a card in place. Erases strategy from the microSD card at /sdcard0/strategy/. Does not erase IP address, configuration data, firmware, or firmware command files from the card. Does not erase data files.

MODBUS CONFIGURATION—READ/WRITE

PR1
RIO
PAC-R
EB
UIO
EIO
SIO
E1
E2
G4EB2

Use this area of the memory map for changing the format of Modbus floats. After you change the format, be sure to store the information to flash using the Status Write area of the device (page 101). The Modbus memory map and information are in the *Modbus/TCP Protocol Guide* (form 1678).

This area is stored to flash.

Starting Address	Length (hex)	Type	Description
FFFF F039 0000	4	UI	Modbus float format (unsigned integer) 0x00000000 = Big Endian 0x00000001 = Big Endian, word swapped. Most significant bit of float is in most significant register.

Last valid address for this area: FFFF F039 0003

NETWORK SECURITY CONFIGURATION—READ/WRITE

PAC-R
PAC-S
EB
SB
UIO
EIO
SIO
LCE
E1
E2
G4EB2

(Does not apply to *groov* I/O units or *groov* RIO modules.) See the *PAC Manager User's Guide* for information on setting up network security for Ethernet-based devices. Also see "FTP User Name/Password Configuration—Read/Write" on page 115.

Starting Address	Length (hex)	Type	Description
FFFF F03A 0004	4	UI	OptoMMP port. Default is 2001.
FFFF F03A 0008	4	UI	Modbus/TCP port. Default is 502.
FFFF F03A 000C	4	UI	(PAC-S, PAC-R, EB, UIO, and EIO only) SNMP port for SNMP agent. Default is 161.
FFFF F03A 0010	4	UI	(PAC-S, PAC-R, EB, UIO, and LCE only; limited use for E1 and E2) FTP port. Default is 21.
FFFF F03A 0020	4	IP	IP Filter Address 0
FFFF F03A 0024	4	IP	IP Filter Mask 0
FFFF F03A 0028	4	IP	IP Filter Address 1
FFFF F03A 002C	4	IP	IP Filter Mask 1
FFFF F03A 0030	4	IP	IP Filter Address 2
FFFF F03A 0034	4	IP	IP Filter Mask 2

Starting Address	Length (hex)	Type	Description
FFFF F03A 0038	4	IP	IP Filter Address 3
FFFF F03A 003C	4	IP	IP Filter Mask 3
FFFF F03A 0040	30	IP	Additional IP Filter Addresses and Filter Masks (4–9)
FFFF F03A 0070	4	UI	Stop incoming broadcasts. 0 = off (default)
FFFF F03A 0074	4	UI	PAC Control host task listen port (TCP). Default: 22001. 0 = Do not listen for commands via TCP.
FFFF F03A 0078	4	UI	Enable/disable EtherNet/IP protocol. 0=disabled; 1=enabled (default)
FFFF F03A 007C	4	UI	Enable/disable HTTPS Web server for SNAP PAC REST API

Last valid address for this area: FFFF F03A 007F

SSI MODULE CONFIGURATION—READ/WRITE

PAC-REB SB

Use this area to configure SSI (serial synchronous interface) modules on the rack. (Does not apply to *groov* I/O units.) The table shows both ports on the first module only; additional modules follow the same pattern, starting on even 100 hex boundaries, with each port starting at even 40 hex boundaries.

Before configuring or using these modules, see the *SNAP SSI (Serial Synchronous Interface) Module User's Guide* (form 1931).

Starting Address	Length (hex)	Type	Description
FFFF F03A 1000	4	UI	Module 0, Port 0: Number of bits in SSI frame (4–32)
FFFF F03A 1004	4	UI	Module 0, Port 0: Clock divider
FFFF F03A 1008	4	UI	Module 0, Port 0: Data delay (clock cycles)
FFFF F03A 100C	4	UI	Module 0, Port 0: Most significant data bit offset (0–28)
FFFF F03A 1010	4	UI	Module 0, Port 0: Data bits in the frame (4–32)
FFFF F03A 1014	4	UI	Module 0, Port 0: Error bit offset within the frame. 0–31 = Offset; –1 = No error bit
FFFF F03A 1018	4	UI	Module 0, Port 0: Error bit meaning. 0=high bit indicates error; 1=low bit indicates error
FFFF F03A 101C	4	UI	Module 0, Port 0: Data coding. 0=binary; 1=Gray code
FFFF F03A 1020	4	UI	Module 0, Port 0: Enable scanning. 0=disabled; 1=enabled
FFFF F03A 1024	1C	–	Pad for alignment
FFFF F03A 1040	4	UI	Module 0, Port 1: Number of bits in SSI frame (4–32)
FFFF F03A 1044	4	UI	Module 0, Port 1: Clock divider
FFFF F03A 1048	4	UI	Module 0, Port 1: Data delay (clock cycles)
FFFF F03A 104C	4	UI	Module 0, Port 1: Most significant data bit offset (0–28)
FFFF F03A 1050	4	UI	Module 0, Port 1: Data bits in the frame (4–32)
FFFF F03A 1054	4	UI	Module 0, Port 1: Error bit offset within the frame. 0–31 = Offset; –1 = No error bit
FFFF F03A 1058	4	UI	Module 0, Port 1: Error bit meaning. 0=high bit indicates error; 1=low bit indicates error
FFFF F03A 105C	4	UI	Module 0, Port 1: Data coding. 0=binary; 1=Gray code
FFFF F03A 1060	4	UI	Module 0, Port 1: Enable scanning. 0=disabled; 1=enabled
FFFF F03A 1064	1C	–	Pad for alignment

Starting Address	Length (hex)	Type	Description
Additional modules follow in order on even 100 hex boundaries.			
FFFF F03A 1F40	40	UI	Module 15, Port 1 Configuration

Last valid address for this area: FFFF F03A 1FFF

SERIAL MODULE IDENTIFICATION—READ ONLY

PAC-REB
UIO
EIO
SIO

Use this area to find out about SNAP serial communication modules on the rack. (Does not apply to *groov* I/O units.) The table shows the first two modules only; additional modules follow the same pattern, starting on even 10 hex boundaries.

For important information on using these modules, see the *SNAP Serial Communication Module User's Guide* (form 1191).

Starting Address	Length (hex)	Type	Description
FFFF F03A 7F00	1	UI	Serial module 0: Module hardware type. 0xF0 = SNAP-SCM-232 *or* SNAP-SCM-232 (Rev A) 0xF1 = SNAP-SCM-485-422 *or* SNAP-SCM-485 0xF6 = SNAP-SCM-PROFI 0xF8 = SNAP-SCM-MCH16 0xF9 = SNAP-SCM-W2 0xFA = SNAP-SCM-SSI 0xFB = SNAP-SCM-ST2 0xFC = SNAP-SCM-CAN2B (These are not serial modules, but use serial for communication): 0x2A = SNAP-AIMA-iH 0xAB - SNAP-AOA-23-iH
FFFF F03A 7F01	1	UI	Serial module 0: Module hardware subtype 0 = Modules manufactured before June 2003 1 = Modules manufactured June 2003 and after
FFFF F03A 7F02	1	UI	Serial module 0: Module hardware revision (month)
FFFF F03A 7F03	1	UI	Serial module 0: Module hardware revision (day)
FFFF F03A 7F04	2	UI	Serial module 0: Module hardware revision (year)
FFFF F03A 7F06	4	UI	Serial module 0: Module hardware loader revision
FFFF F03A 7F0A	4	UI	Serial module 0: Module hardware firmware revision
FFFF F03A 7F0E	2	–	Pad for alignment
FFFF F03A 7F10	1	UI	Module 1: Module hardware type
FFFF F03A 7F11	1	UI	Module 1: Module hardware subtype
FFFF F03A 7F12	1	UI	Module 1: Module hardware revision (month)
FFFF F03A 7F13	1	UI	Module 1: Module hardware revision (day)
FFFF F03A 7F14	2	UI	Module 1: Module hardware revision (year)
FFFF F03A 7F16	4	UI	Module 1: Module hardware loader revision
FFFF F03A 7F1A	4	UI	Module 1: Module hardware firmware revision
FFFF F03A 7F1E	2	–	Pad for alignment

Additional modules follow in order on even 10 hex boundaries.

Last valid address for this area: FFFF F03A 7FFA

SERIAL MODULE CONFIGURATION—READ/WRITE

PAC-R
EB
UIO
EIO
SIO

Use this area to configure SNAP serial communication modules on the rack. (Does not apply to *groov* I/O units.) Only two ports—the ports for a serial module in position 0 on the rack—are shown in the table. (SNAP-SCM-PROFI, SNAP-SCM-MCH16, and SNAP-SCM-CAN2B modules have only one port, port A.) Ports for modules in other positions on the rack follow the same pattern and start on even 10 hex boundaries. See the table on page 108 for a list of module and port numbers.

For important information on using these modules, see the *SNAP Serial Communication Module User's Guide* (form 1191). For the SNAP-SCM-MCH16, see the *SNAP PAC Motion Control Subsystem User's Guide* (form 1673).

Starting Address	Length (hex)	Type	Description
FFFF F03A 8000	4	UI	Port A on serial module in position 0 on the rack: TCP port number for access to serial port. Default is 22500.
FFFF F03A 8004	4	UI	Port A, position 0: Baud rate
FFFF F03A 8008	1	UI	Port A, position 0: Parity. None = 0x4E; even = 0x45; odd = 0x4F SNAP-SCM-PROFI and SNAP-SCM-MCH16 = even (0x45)
FFFF F03A 8009	1	UI	Port A, position 0: Data Bits SNAP-SCM-PROFI = 7; SNAP-SCM-MCH16 = 8 only.
FFFF F03A 800A	1	UI	Port A, position 0: Stop Bits. SNAP-SCM-PROFI = 1
FFFF F03A 800B	1	UI	Port A, position 0: Hardware flow control. 1 = Yes, 0 = No
FFFF F03A 800C	1	UI	Port A, position 0: Send test message on powerup 1 = Yes; 0 = No
FFFF F03A 800D	3	–	Pad for alignment
FFFF F03A 8010	4	UI	Port B on serial module in position 0 on the rack: TCP port number for access to serial port. Default is 22501.
FFFF F03A 8014	4	UI	Port B, position 0: Baud rate
FFFF F03A 8018	1	UI	Port B, position 0: Parity
FFFF F03A 8019	1	UI	Port B, position 0: Data Bits
FFFF F03A 801A	1	UI	Port B, position 0: Stop Bits
FFFF F03A 801B	1	UI	Port B, position 0: Hardware flow control. 1 = Yes, 0 = No
FFFF F03A 801C	1	UI	Port B, position 0: Send test message on powerup
FFFF F03A 801D	3	–	Pad for alignment
Additional ports follow in order on even 10 hex boundaries. See port table, below.			
FFFF F03A 8200	4	UI	Port A, position 0: End-of-message (EOM) characters. The device can check any one of up to four characters as the EOM indicator. [Example: 0x0D0A0000 looks for a 13 (hex 0D) or 10 (hex 0A)] EOM checking occurs only when using the serial module port with serial events. Max. message size = 250 bytes (Messages that exceed 249 bytes are received as 249-byte chunks followed by a smaller chunk containing all characters up to the EOM character.)
FFFF F03A 8204	C	–	Pad for alignment
FFFF F03A 8210	4	UI	Port B, position 0: End-of-message characters.
Additional ports follow in order on even 10 hex boundaries.			
FFFF F03A 8400	1	UI	Position 0: Module mode of operation (0 = 2-wire; 1 = 4-wire) SNAP-SCM-PROFI =2-wire (0).
FFFF F03A 8401	1	UI	Position 1: Module mode of operation (0 = 2-wire; 1 = 4-wire) SNAP-SCM-PROFI =2-wire (0).
Additional modules follow in order.			
Last valid address for this area: FFFF F03A 840F			

Serial Module and Port Numbers

PAC-REB
UIO
EIO
SIO

For quick reference, the following table shows serial modules and ports, their default TCP port numbers, and their starting memory map addresses, beginning with FFFF F03A 8000. (Does not apply to *groov* I/O units.) Remember that SNAP-SCM-PROFI, SNAP-SCM-MCH16, and SNAP-SCM-CAN2B modules have only one port, Port A.

Module	Port	Default TCP Port	Memory Map Address
0	A	22500	8000
0	B	22501	8010
1	A	22502	8020
1	B	22503	8030
2	A	22504	8040
2	B	22505	8050
3	A	22506	8060
3	B	22507	8070
4	A	22508	8080
4	B	22509	8090
5	A	22510	80A0
5	B	22511	80B0
6	A	22512	80C0
6	B	22513	80D0
7	A	22514	80E0
7	B	22515	80F0

Module	Port	Default TCP Port	Memory Map Address
8	A	22516	8100
8	B	22517	8110
9	A	22518	8120
9	B	22519	8130
10	A	22520	8140
10	B	22521	8150
11	A	22522	8160
11	B	22523	8170
12	A	22524	8180
12	B	22525	8190
13	A	22526	81A0
13	B	22527	81B0
14	A	22528	81C0
14	B	22529	81D0
15	A	22530	81E0
15	B	22531	81F0

WIEGAND SERIAL MODULE CONFIGURATION—READ/WRITE

PAC-REB
UIO
EIO

(Does not apply to *groov* I/O units or SNAP Simple I/O) Use this area to configure SNAP Wiegand serial communication modules on the rack. Only a few modules and ports are shown in the table. Other ports and modules on the rack follow the same pattern. See the table on page 109 for a list of module and port numbers.

For important information on using these modules, see the *SNAP Serial Communication Module User's Guide* (form 1191).

Starting Address	Length (hex)	Type	Description
FFFF F03A 8500	4	UI	Wiegand module 0: Loader version number
FFFF F03A 8504	4	UI	Wiegand module 0: Firmware (kernel) version number
FFFF F03A 8508	4	UI	Wiegand module 1: Loader version number
FFFF F03A 850C	4	UI	Wiegand module 1: Firmware (kernel) version number
Modules 2–15 follow in order.			
FFFF F03A 8600	4	UI	Port A on Wiegand module in position 0 on the rack: TCP port number for access to serial port. Default is 22500.
FFFF F03A 8604	4	UI	Port A, position 0: Data format (O for Opto format, 26, 30, 32, 34, 35, 36, 37, 40, or C for custom format)
FFFF F03A 8608	4	UI	Port A, position 0: Total Length (hex) of data in the transmission

Starting Address	Length (hex)	Type	Description
FFFF F03A 860C	4	UI	Port A, position 0: First bit of the site code
FFFF F03A 8610	4	UI	Port A, position 0: Length of the site code, in bits
FFFF F03A 8614	4	UI	Port A, position 0: First bit of the badge code (should be the next bit after the site code)
FFFF F03A 8618	4	UI	Port A, position 0: Length of the badge code, in bits
FFFF F03A 861C	24	–	Pad for alignment
FFFF F03A 8640	4	UI	Port B on Wiegand module in position 0 on the rack: TCP port number for access to serial port. Default is 22501.
FFFF F03A 8644	4	UI	Port B, position 0: Data format (O for Opto format, 26, 30, 32, 34, 35, 36, 37, 40, or C for custom format)
FFFF F03A 8648	4	UI	Port B, position 0: Total length of data in the transmission
FFFF F03A 864C	4	UI	Port B, position 0: First bit of the site code
FFFF F03A 8650	4	UI	Port B, position 0: Length of the site code, in bits
FFFF F03A 8654	4	UI	Port B, position 0: First bit of the badge code (should be the next bit after the site code)
FFFF F03A 8658	4	UI	Port B, position 0: Length of the badge code, in bits
FFFF F03A 865C	24	–	Pad for alignment

Additional ports follow in order on even 40 hex boundaries. See table on the next page.

Last valid address for this area: FFFF F03A 8DC3

Wiegand Module and Port Numbers

PAC-REB UIO EIO

For quick reference, the following table shows Wiegand modules and ports, their default TCP port numbers, and their starting memory map addresses, beginning with FFFF F03A 8600. (Does not apply to *groov* I/O units.)

Module	Port	Default TCP port	Memory Map Address
0	A	22500	8600
0	B	22501	8640
1	A	22502	8680
1	B	22503	86C0
2	A	22504	8700
2	B	22505	8740
3	A	22506	8780
3	B	22507	87C0
4	A	22508	8800
4	B	22509	8840
5	A	22510	8880
5	B	22511	88C0
6	A	22512	8900
6	B	22513	8940
7	A	22514	8980
7	B	22515	89C0

Module	Port	Default TCP port	Memory Map Address
8	A	22516	8A00
8	B	22517	8A40
9	A	22518	8A80
9	B	22519	8AC0
10	A	22520	8B00
10	B	22521	8B40
11	A	22522	8B80
11	B	22523	8BC0
12	A	22524	8C00
12	B	22525	8C40
13	A	22526	8C80
13	B	22527	8CC0
14	A	22528	8D00
14	B	22529	8D40
15	A	22530	8D80
15	B	22531	8DC0

SNAP-SCM-CAN2B SERIAL MODULE CONFIGURATION—READ/WRITE

PAC-REB

Use this area to configure SNAP-SCM-CAN2B serial communication modules on the rack. (Does not apply to *groov* I/O units.) Each module has only one port. Only two modules are shown in the table; others on the rack follow the same pattern. See the table on page 109 for a list of module and port numbers.

If the Data Masks and Filters are all set to 0, then all CAN packets will be received. If you want the SNAP-SCM-CAN2B module to provide filtering, then configure the Data Masks and Filters. Always start with the highest priority mask and filter, Data Mask 0 and Filter 0. See additional information in "CAN Packet Table" on page 111.

For important information on using these modules, see the *SNAP Serial Communication Module User's Guide* (form 1191) and the *SNAP-SCM-CAN2B Module* data sheet (form 1537).

Starting Address	Length (hex)	Type	Description
FFFF F03A 9000	4	UI	Module 0: TCP/UDP Port Number.
FFFF F03A 9004	4	UI	Module 0: BAUD Rate. Supports 1000000, 500000, 250000, 125000, 100000, 50000, 20000, 10000 bps
FFFF F03A 9008	4	UI	Module 0: Data Mask 0 for Filters 0 and 1. This mask determines which bits in the CAN ID are examined. If any mask bit is set to a zero, that bit will automatically be accepted, regardless of the filter bit. See truth table below.
FFFF F03A 900C	4	UI	Module 0: Filter 0. Highest priority filter. See truth table below.
FFFF F03A 9010	4	UI	Module 0: Filter 1. If filter value is 0, unused, then Filter 0 will be used instead. See truth table below.
FFFF F03A 9014	4	UI	Module 0: Data Mask 1 for Filters 2, 3, 4, and 5. This mask determines which bits in the CAN ID are examined. If any mask bit is set to a zero, that bit will automatically be accepted, regardless of the filter bit. See truth table below. If mask is 0, unused, then Data Mask 0 will be used instead.
FFFF F03A 9018	4	UI	Module 0: Filter 2. If filter is 0, unused, then Filter 1 will be used instead. See truth table below.
FFFF F03A 901C	4	UI	Module 0: Filter 3. If filter is 0, unused, then Filter 2 will be used instead. See truth table below.
FFFF F03A 9020	4	UI	Module 0: Filter 4. If filter is 0, unused, then Filter 3 will be used instead. See truth table below.
FFFF F03A 9024	4	UI	Module 0: Filter 5. If filter is 0, unused, then Filter 4 will be used instead. Lowest priority filter. See truth table below.
FFFF F03A 9028	4	UI	Module 0: Error Code. For a SNAP-SCM-CAN2B using receive only, reports any errors it encounters. See Error Code table on page 111. Does NOT apply to SNAP-SCM-CAN2B using receive/transmit. See page 111.
FFFF F03A 902C	4	UI	Module 1: TCP/UDP Port Number.
FFFF F03A 9030	4	UI	Module 1: BAUD Rate. Supports 1000000, 500000, 250000, 125000, 100000, 50000, 20000, 10000 bps
FFFF F03A 9034	4	UI	Module 1: Data Mask 0 for Filters 0 and 1. This mask determines which bits in the CAN ID are examined. If any mask bit is set to a zero, that bit will automatically be accepted, regardless of the filter bit. See truth table below.
FFFF F03A 9038	4	UI	Module 1: Filter 0. Highest priority filter. See truth table below.
FFFF F03A 903C	4	UI	Module 1: Filter 1. If filter value is 0, unused, then Filter 0 will be used instead. See truth table below.

Starting Address	Length (hex)	Type	Description
FFFF F03A 9040	4	UI	Module 1: Data Mask 1 for Filters 2, 3, 4, and 5. This mask determines which bits in the CAN ID are examined. If any mask bit is set to a zero, that bit will automatically be accepted, regardless of the filter bit. See truth table below. If mask is 0, unused, then Data Mask 0 will be used instead.
FFFF F03A 9044	4	UI	Module 1: Filter 2. If filter is 0, unused, then Filter 1 will be used instead. See truth table below.
FFFF F03A 9048	4	UI	Module 1: Filter 3. If filter is 0, unused, then Filter 2 will be used instead. See truth table below.
FFFF F03A 904C	4	UI	Module 1: Filter 4. If filter is 0, unused, then Filter 3 will be used instead. See truth table below.
FFFF F03A 9050	4	UI	Module 1: Filter 5. If filter is 0, unused, then Filter 4 will be used instead. Lowest priority filter. See truth table below.
FFFF F03A 9054	4	UI	Module 1: Error Code. Where the SNAP-SCM-CAN2B reports any errors it encounters. See Error Code table below. Related to LED 4 above.

Additional modules follow in order on even 2C hex boundaries. See table on page 112.

Last valid address for this area: FFFF F03A 92BF

CAN Packet Table

The table below shows how CAN packets are accepted or rejected. It applies to memory map addresses for Data Masks and Filters. X = Don't care; so, for example, if you want to receive CAN ID 0x00***FF05***00 and only care about the part in bold, then set your Mask to 0x00FFFF00 and your Filter to 0x00FF0500.

Data Mask Bit	Filter Bit	CAN ID Bit	Accept/Reject
0	X	X	Accept
1	0	0	Accept
1	0	1	Reject
1	1	0	Reject
1	1	1	Accept

CAN Error Codes

The SNAP-SCM-CAN2B keeps track of how many errors have occurred. Possible errors are CRC Error, Acknowledge Error, Form Error, Bit Error, and Stuff Error. If one of these errors is detected, LED 4 is lit and the error counter is incremented.

If you are using the module in receive/transmit mode, use the subroutine from the PAC-INT-CAN-RXTX integration kit (available for free on our website, opto22.com) to send an "S" command, get error information, and clear the errors. Do not use the Error Code memory map address nor the table below, as they are deprecated for receive/transmit. Use the "S" command instead. This command gives you much more information.

If you are using the module in receive-only mode (no transmit), read the returned error codes in the memory map. To clear the error condition in the module, read the Error Code memory map address (0xF03A9028 for module 0). The table below defines the error codes returned in this address:

Error Code	Description
0	Error—Active State. The SNAP-SCM-CAN2B has received less than 96 errors.
-1	Error—Active State. The SNAP-SCM-CAN2B has received 96 or more errors but less than 128 errors.

Error Code	Description
-2	Receiver Overflow. A CAN packet was dropped. This error occurs if the SNAP-SCM-CAN2B can't keep up with the traffic on the CAN bus.
-3	Error—Passive State. The SNAP-SCM-CAN2B has received 128 or more errors but less than 255 errors.
-4	Bus—Off State. The SNAP-SCM-CAN2B has received 255 or more errors. CAN packets can neither be received nor transmitted.

PAC-R EB

SNAP-SCM-CAN2B Module and Port Numbers

For quick reference, the following table shows SNAP-SCM-CAN2B modules and ports, their default TCP port numbers, and their starting memory map addresses, beginning with FFFF F03A 9000. (Does not apply to *groov* I/O units.) Each module has only one port, Port A.

Module	Port	Default TCP port	Memory Map Address
0	A	22500	0xF03A9000
1	A	22502	0xF03A902C
2	A	22504	0xF03A9058
3	A	22506	0xF03A9084
4	A	22508	0xF03A90B0
5	A	22510	0xF03A90DC
6	A	22512	0xF03A9108
7	A	22514	0xF03A9134

Module	Port	Default TCP port	Memory Map Address
8	A	22516	0xF03A9160
9	A	22518	0xF03A918C
10	A	22520	0xF03A91B8
11	A	22522	0xF03A91E4
12	A	22524	0xF03A9210
13	A	22526	0xF03A923C
14	A	22528	0xF03A9268
15	A	22530	0xF03A9294

HART MODULE CONFIGURATION—READ/WRITE

PAC-R EB

Use this area to configure HART SNAP I/O modules on the rack (part numbers SNAP-AIMA-iH and SNAP-AOA-23-iH). (Does not apply to *groov* I/O units.) These analog modules communicate with HART-compatible devices by sending HART protocol communications as serial data over the 4–20 mA analog signal.

Port A is channel 0 on the module; Port B is channel 1. Only the first module is shown in the table. Other modules on the rack follow the same pattern. See the table on page 113 for port numbers and starting addresses for each module and port.

For important information on using these modules, see the HART SNAP I/O Modules User's Guide (form 2132).

Starting Address	Length (hex)	Type	Description
FFFF F03A 9400	4	UI	Port A on module in position 0 on the rack: TCP Port Number. See table on page 113.
FFFF F03A 9404	4	UI	Port A, position 0: Master Address. 0 = Secondary Master, 1 = Primary Master (Default: 1) Use 1 if you want the HART SNAP I/O module to be the permanent master; you can temporarily attach another master device for configuration or troubleshooting.
FFFF F03A 9408	4	UI	Port A, position 0: Retry Limit. Valid values: 0 to 5 (Default: 2) If the module does not receive a valid response from the slave device after the maximum number of retries, it reports an error.

Starting Address	Length (hex)	Type	Description
FFFF F03A 940C	4	UI	Port A, position 0: Burst Mode. 0 = Don't report burst messages, 1 = Report burst messages Burst messages occur when a slave device in a special mode sends data without a request from a master.
FFFF F03A 9410	4	UI	Port A, position 0: Promiscuous Mode. 0 = Don't report other master requests/responses, 1 = Report other master requests/responses 1 means that the module will report transactions initiated by the other master, including requests and responses.
FFFF F03A 9414	4	UI	Port A, position 0: Preamble Count. Valid values: 5 to 20 (Default: 5) Older HART devices may require more than 5 preamble characters. Verify using HART command 0.
FFFF F03A 9418	18	UI	Port A, position 0: Pad for alignment
FFFF F03A 9430	4	UI	Port B, position 0: TCP Port Number. See table on page 113.
FFFF F03A 9434	4	UI	Port B, position 0: Master Address. 0 = Secondary Master, 1 = Primary Master (Default: 1) Use 1 if you want the HART SNAP I/O module to be the permanent master; you can temporarily attach another master device for configuration or troubleshooting.
FFFF F03A 9438	4	UI	Port B, position 0: Retry Limit. 0 to 5 (Default: 2) If the module does not receive a valid response from the slave device after the maximum number of retries, it reports an error.
FFFF F03A 943C	4	UI	Port B, position 0: Burst Mode. 0 = Don't report burst messages, 1 = Report burst messages Burst messages occur when a slave device in a special mode sends data without a request from a master.
FFFF F03A 9440	4	UI	Port B, position 0: Promiscuous Mode. 0 = Don't report other master requests/responses, 1 = Report other master requests/responses 1 means that the module will report transactions initiated by the other master, including requests and responses.
FFFF F03A 9444	4	UI	Port B, position 0: Preamble Count. 5 to 20 (Default: 5) Older HART devices may require more than 5 preamble characters. Verify using HART command 0.
FFFF F03A 9448	18	UI	Port B, position 0: Pad for alignment

Additional ports and modules follow in order, ports on 30 hex boundaries and modules on 60 hex boundaries. See "HART Module and Port Numbers," below.

Last valid address for this area: FFFF F03A 99FF

HART Module and Port Numbers

PAC-REB SB

For quick reference, the following table shows HART modules and ports, their default TCP port numbers, and their starting memory map addresses, beginning with FFFF F03A 9400. (Does not apply to *groov* I/O units.)

Module	Port	Default TCP port	Memory Map Address
0	A	22500	9400
0	B	22501	9430
1	A	22502	9460
1	B	22503	9490
2	A	22504	94C0
2	B	22505	94F0

Module	Port	Default TCP port	Memory Map Address
8	A	22516	9700
8	B	22517	9730
9	A	22518	9760
9	B	22519	9790
10	A	22520	97C0
10	B	22521	97F0

Module	Port	Default TCP port	Memory Map Address
3	A	22506	9520
3	B	22507	9550
4	A	22508	9580
4	B	22509	95B0
5	A	22510	95E0
5	B	22511	9610
6	A	22512	9640
6	B	22513	9670
7	A	22514	96A0
7	B	22515	96D0

Module	Port	Default TCP port	Memory Map Address
11	A	22522	9820
11	B	22523	9850
12	A	22524	9880
12	B	22525	98B0
13	A	22526	98E0
13	B	22527	9910
14	A	22528	9940
14	B	22529	9970
15	A	22530	99A0
15	B	22531	99D0

SNMP CONFIGURATION—READ/WRITE

PAC-R
PAC-S
EB
UIO
EIO
G4EB2

(Does not apply to *groov* I/O units, *groov* RIO modules, or SNAP Simple I/O) Use this area to configure SNMP if you are sending messages to an enterprise management system, such as Computer Associates' Unicenter TNG® or Hewlett Packard's Open View®, using the Simple Network Management Protocol. For more information on using SNMP, see page 49.

Starting Address	Length (hex)	Type	Description
FFFF F03C 0000	20	S-ZT	sysName—the name assigned to the SNAP device as a managed node within the SNMP management system
FFFF F03C 0020	20	S-ZT	sysLocation—the physical location of the device
FFFF F03C 0040	20	S-ZT	sysContact—the ID of the contact person for the device
FFFF F03C 0060	4	UI	Enable authentication trap. Yes = 1; No = 0. Default is 0.
FFFF F03C 0064	4	UI	Enable cold start trap. Yes = 1; No = 0. Default is 0.
FFFF F03C 0068	14	S-ZT	Community 1: Name of community (string)
FFFF F03C 007C	4	UI	Community 1: Set read access privileges. Yes = 1; No = 0. Default is 0.
FFFF F03C 0080	4	UI	Community 1: Set write access privileges. Yes = 1; No = 0. Default is 0.
FFFF F03C 0084	4	UI	Community 1: Set trap access privileges. Yes = 1; No = 0. Default is 0.
FFFF F03C 0088	14	S-ZT	Community 2: Name of community (string)
FFFF F03C 009C	4	UI	Community 2: Set read access privileges. Yes = 1; No = 0. Default is 0.
FFFF F03C 00A0	4	UI	Community 2: Set write access privileges. Yes = 1; No = 0. Default is 0.
FFFF F03C 00A4	4	UI	Community 2: Set trap access privileges. Yes = 1; No = 0. Default is 0.
Communities 3–8 follow in order.			
FFFF F03C 0168	14	S-ZT	Host 1: Name of community host belongs to (string)
FFFF F03C 017C	4	IP	Host 1: IP address
FFFF F03C 0180	14	S-ZT	Host 2: Name of community host belongs to (string)

Starting Address	Length (hex)	Type	Description
FFFF F03C 0194	4	IP	Host 2: IP address
FFFF F03C 0198	14	S-ZT	Host 3: Name of community host belongs to (string)
FFFF F03C 01AC	4	IP	Host 3: IP address
Hosts 4–16 follow in order.			
FFFF F03C 0308	4	UI	SNMP trap destination port. Default is 162.
FFFF F03C 030C	4	UI	SNMP trap version: 0 = agent sends SNMPv1 traps; 1 = agent sends SNMPv2 notifications. Default = 0. Affects all traps/notifications; takes effect immediately.
Last valid address for this area: FFFF F03C 030B			

FTP USER NAME/PASSWORD CONFIGURATION—READ/WRITE

PAC-R
PAC-S
EB
G4EB2

Use this area to configure the user name and password for FTP use. (Does not apply to *groov* I/O or RIO units.) For more information on using FTP and the controller or brain's file system, see the *PAC Manager User's Guide*.

Starting Address	Length (hex)	Type	Description
FFFF F03D 0000	40	S-ZT	User name for FTP server access
FFFF F03D 0040	40	S-ZT	Password for FTP server access
Last valid address for this area: FFFF F03D 0079			

PPP CONFIGURATION—READ/WRITE

PAC-R
PAC-S
UIO
EIO
LCE

Use this area to configure PPP if you are communicating with the controller or brain via a modem connection. (Does not apply to *groov* I/O or RIO units.) For more information on setting up PPP, see the *PAC Manager User's Guide*.

Starting Address	Length (hex)	Type	Description
FFFF F03E 0000	4	IP	Local IP address for PPP interface. Default is 192.168.0.1
FFFF F03E 0004	4	IP	Remote IP address. This IP address is assigned to devices that connect to the brain or controller and request an IP address. *This address must be on the same subnet as the Local IP address.* Default is 192.168.0.2
FFFF F03E 0008	4	UI	Serial port speed. Default is 19,200 bps.
FFFF F03E 000C	4	UI	Serial port parity. Default is none. None = 0x10; even = 0x4; odd = 0x0
FFFF F03E 0010	4	UI	Serial port stop bits. Possible values: 1 or 2. Default is 1.
FFFF F03E 0014	4	UI	Serial port data bits. Possible values: 6–8. Default is 8.
FFFF F03E 0018	40	S-ZT	Modem initialization string (null terminated). This string is sent to the modem once when the brain or controller boots. The modem must be configured to **ignore DTR** and **use no flow control**. The modem is reset (ATZ) between each call. We suggest that settings be saved to a profile in the modem's NVRAM and the modem configured to load that profile every time it is reset. The modem initialization string can be used to perform this task whenever the brain or controller powers up. See the device's user's guide for more information. Default is: AT&D0^M~~~~

Starting Address	Length (hex)	Type	Description
FFFF F03E 0058	4	IP	Subnet mask for Local IP address. Default is 0.0.0.0—Required only if you are using classless IP addressing. If not, leave it at 0 and the brain or controller will calculate the appropriate subnet from the Local IP address.
FFFF F03E 005C	4	UI	Maximum number of times PPP will retry to authenticate a link. Default is 3.
FFFF F03E 0060	4	UI	Serial port flow control. 0 = none; 1 = hardware (RTS/CTS)
FFFF F03E 0064	40	S-ZT	Modem hangup string. This string is sent by the brain or controller to the modem when it wants the modem to hang up. (Note: A ^t in this string forces an LCP terminate request packet in a PPP frame to be sent, which can be useful to force packet-switched data devices with a local PPP interface to hang up and enter command mode.) Default is: ~~~+++~~~ATH0^M~~~
FFFF F03E 00A4	4	UI	(PAC-S and PAC-R only) Send commands to the PPP service: 0 = None 1 = Start PPP service. If PPP is Disabled, rereads all PPP configuration settings and starts the service. Check PPP status in F03EB800. 2 = Stop PPP service. Applies only if PPP is not disabled. Read F03EB800 to monitor shutdown progress. 3 = Start outgoing link. Applies only if PPP is Idle or Listening (see F03EB800). Starts an outgoing PPP connection. 4 = Stop link. Applies only if PPP status is Outgoing Connected or Incoming Connected (see F03EB800). Closes the PPP link.
FFFF F03E 00A8	4	UI	Echo request period (in seconds). Default = 10 s.
FFFF F03E 00AC	4	UI	Echo request retries. Default = 3.
FFFF F03E 00B0	4	UI	Connection establishment timeout (in seconds). Default = 60 s.
Last valid address for this section: FFFF F03E 00B3			
FFFF F03E 6000	4	UI	Enable PPP for incoming calls. Default is 0. Enable = 1, Disable = 0
FFFF F03E 6004	4	UI	Set default gateway to PPP interface. Default is 0. Yes = 1, No = 0. If enabled, all IP packets addressed to destinations that are not on the same subnet as the Ethernet interface will be sent out the PPP interface. Enable this only when the remote device can route packets to their ultimate destination. The setting is in effect only when an incoming PPP session is active.
FFFF F03E 600C	40	S-ZT	Modem listen string (null terminated). Default is: ATS0=1^M~" Prior to waiting for a call, the brain or controller resets the modem and sends this string to it. The string is sent every time the brain or controller prepares to listen for a call.
FFFF F03E 604C	4	UI	Inactivity timeout. Number of seconds an incoming link can remain idle before the link is closed. Default is 30.
FFFF F03E 6050	10	S-ZT	(Applies to SNAP firmware R5.0 and older[a]) Login (null terminated). Login name for authentication on incoming PPP sessions.
FFFF F03E 6060	10	S-ZT	(Applies to SNAP firmware R5.0 and older[a]) Password (null terminated). Password for authentication on incoming PPP sessions.
FFFF F03E 6070	40	S-ZT	(Applies to SNAP firmware R5.1 and newer[a]) Login (null terminated). Login name for authentication on incoming PPP sessions.
FFFF F03E 60B0	40	S-ZT	(Applies to SNAP firmware R5.1 and newer[a]) Password (null terminated). Password for authentication on incoming PPP sessions.
Last valid address for this section: FFFF F03E 60EF			

Starting Address	Length (hex)	Type	Description
FFFF F03E B000	4	UI	Enable PPP for outgoing calls (dial on demand). Enable = 1; disable = 0. Default is 0.
FFFF F03E B004	4	UI	Specify local IP address. Yes = 1; No = 0. Default is 0. For outgoing calls, the brain or controller can either specify the IP address it wants to use (entered in FFFF F03E 0000) or ask the remote device to assign an address.
FFFF F03E B008	4	UI	Set default gateway to PPP interface. Yes = 1; No = 0. Default is 0. If enabled, all IP packets addressed to destinations that are not on the same subnet as the Ethernet interface will be sent out the PPP interface. Enable this only when the remote device can route packets to their ultimate destination. The setting is in effect only when an outgoing PPP session is active.
FFFF F03E B00C	4	–	Reserved
FFFF F03E B010	10	S-ZT	(Applies to SNAP firmware R5.0 and older[a]) Login (null terminated). Login name for authentication on outgoing PPP sessions.
FFFF F03E B020	10	S-ZT	(Applies to SNAP firmware R5.0 and older[a]) Password (null terminated). Password for authentication on outgoing PPP sessions.
FFFF F03E B030	4		PPP inactivity timeout in seconds. Default is 30. If the brain or controller sends no traps for this number of seconds after the PPP session is negotiated, the modem will hang up. A zero in this field disables the timer.
FFFF F03E B034	40	S-ZT	Phone number to dial for outgoing PPP connections (null terminated).
FFFF F03E B074	4	UI	Maximum connection time in seconds. Default is 0 (disabled). Maximum amount of time an outgoing PPP connection can stay connected after successful negotiation.
FFFF F03E B078	4	UI	Maximum number of times the brain or controller will try redialing if the first attempt fails. Default is 0.
FFFF F03E B07C	4	UI	Retry interval in seconds. Default is 0. Number of seconds the brain or controller will wait before trying to redial after the first attempt fails.
FFFF F03E B080	4	UI	Disable time in seconds. Default is 0. If the maximum connect time or maximum number of retries has been reached, the outgoing PPP dialer waits this long before doing anything.
FFFF F03E B084	4	UI	Link always connected for outgoing PPP. If always connected, brain or controller dials out only on powerup and anytime the PPP link goes down. Default is 0 (not always connected). 0 is used for most applications that use circuit-switched data service to communicate. 1 is used for most applications that use packet-switched data service.
FFFF F03E B088	40	S-ZT	(Applies to SNAP firmware R5.1 and newer[a]) Login (null terminated). Login name for authentication on outgoing PPP sessions.
FFFF F03E B0C8	40	S-ZT	(Applies to SNAP firmware R5.1 and newer*) Password (null terminated). Password for authentication on outgoing PPP sessions.

[a] Changed login and password addresses: As of SNAP firmware version 5.1, login and password were lengthened to 0x40 bytes. Applications using the old memory map addresses will still work, as values will be read from the old addresses and stored to the new addresses. To take advantage of the longer login and password, however, you need to change your application to use the new addresses.

Last valid address for this area: FFFF F03E B107

PPP STATUS—READ ONLY

PAC-R
PAC-S
UIO
EIO
LCE

Use this area to check status on Point-to-Point Protocol (PPP) communication using a modem. (Does not apply to *groov* I/O units or *groov* RIO modules.)

Starting Address	Length (hex)	Type	Description
FFFF F03E B800	4	UI	Connection status (differs for SNAP devices: EIO: 0 - Idle 1 - Connecting 2 - Listening 3 - Connected 4 - Disconnecting 5 - Disconnected PAC-S, LCE, and UIO: 0 - Idle 1 - Outgoing Connecting 2 - Outgoing Connected 3 - Outgoing Disconnecting 4 - Listening 5 - Incoming Connecting 6 - Incoming Connected 7 - Incoming Disconnecting 8 - Shutting Down 9 - Disabled
FFFF F03E B804	4	UI	Connection type: 0 - Outgoing; 1 - Incoming; 2 - None
FFFF F03E B808	4	UI	Number of retries (times the outgoing dialer has tried to dial out). When this number reaches the number configured in F03E B078 as the maximum number of retries, the disable timer starts running and the outgoing dialer stops dialing until the disable timer expires
FFFF F03E B80C	4	UI	Number of milliseconds left on the idle timer before it expires and closes the connection. 0 = disabled. Activity on the PPP link resets the idle timer to 1000 times the value in F03E B030 for outgoing connections or F03E 604C for incoming connections. This timer limits the duration of a PPP link with no activity.
FFFF F03E B810	4	UI	Number of milliseconds left on the retry timer before the outgoing dialer tries to dial out again. The retry timer starts running when an outgoing dial attempt fails. Its initial value is the value configured in F03E B07C.
FFFF F03E B814	4	UI	Number of milliseconds left on the disable timer. While the disable timer is active, the outgoing dialer is prevented from dialing out. Initial value is the value configured in F03E B080.
FFFF F03E B818	4	UI	Number of milliseconds left on the outgoing connect timer. This timer limits the length of an outgoing PPP connection regardless of activity. When an outgoing PPP link is established, this timer is set to the value configured in F03E B074. When the timer expires, the outgoing PPP link is terminated and the disable timer is started.
FFFF F03E B81C	4	UI	Number of buffered outgoing frames waiting for a PPP link to be established.
FFFF F03E B820	4	UI	UART TX buffer overruns. Number of bytes of transmit data that were dropped because the modem was not ready to receive it. The brain or controller waits for up to one second for the modem to be ready. After that, the brain or controller drops one byte of transmit data and flags the modem internally as offline. When the device has another byte of transmit data to send, it checks once to see if the modem is ready to receive it; if not, it drops the byte. If the modem is ready, the device sends the data and flags the modem internally as online.
FFFF F03E B824	4	IP	Current local IP address (SNAP Ultimate and SNAP-LCE only). Current IP address assigned to the PPP interface by a remote peer; valid only while the PPP link is connected. Applies only If outgoing PPP is configured not to specify its local IP address.

Last valid address for this area: FFFF F03F FFFF

STREAMING CONFIGURATION—READ/WRITE

PR1
RIO
PAC-R
EB
UIO
EIO
SIO
G4EB2

Use this area to configure data streaming from the I/O unit to a host. For more information, see page 51. This area is stored to flash.

Starting Address	Length (hex)	Type	Description
FFFF F03F FFC0	4	–	Reserved
FFFF F03F FFC4	4	B	Enable or disable I/O mirroring (Boolean) 0 = disable; non-0 = enable
FFFF F03F FFC8	4	UI	Beginning address of the data you want to stream. Do not use if you are streaming the entire streaming section shown on page 138. Use only to stream a portion of the streaming section or some other portion of the memory map.
FFFF F03F FFCC	4	UI	Size of data to stream. Do not use if you are streaming the entire streaming section shown on page 138. Use only to stream a portion of the streaming section or some other portion of the memory map. Maximum data size: 1480 bytes.
FFFF F03F FFD0	4	B	Streaming On/Off (Boolean). 0 = off; non-0 = on.
FFFF F03F FFD4	4	UI	Streaming Interval, in milliseconds (unsigned integer)
FFFF F03F FFD8	4	UI	UDP port number to stream to
FFFF F03F FFDC	4	–	Reserved
FFFF F03F FFE0	4	IP	Stream target IP address #1
FFFF F03F FFE4	4	IP	Stream target IP address #2
FFFF F03F FFE8	4	IP	Stream target IP address #3
FFFF F03F FFEC	4	IP	Stream target IP address #4
FFFF F03F FFF0	4	IP	Stream target IP address #5
FFFF F03F FFF4	4	IP	Stream target IP address #6
FFFF F03F FFF8	4	IP	Stream target IP address #7
FFFF F03F FFFC	4	IP	Stream target IP address #8

Last valid address for this area: FFFF F03F FFFF

DIGITAL BANK READ—READ ONLY

PAC-R
EB
SB
UIO
EIO
SIO
E1
G4EB2

Applies to most digital modules. (Does not apply to *groov* I/O units, *groov* RIO modules, or SNAP high-density digital modules; instead, see "High-Density Digital—Read Only" on page 147.)

For help in interpreting data, see "Mask Data" on page 58. For general information on using counters, see page 33.

Starting Address	Length (hex)	Type	Description
FFFF F040 0000	8	M	State of digital channels (mask)
FFFF F040 0008	8	M	State of on-latches (mask)
FFFF F040 0010	8	M	State of off-latches (mask)
FFFF F040 0018	8	M	Active counters (mask)
FFFF F040 0020	4	M	Reserved for completion of pulse measurement or one-time frequency or period measurement on digital channels 32–63

Starting Address	Length (hex)	Type	Description
FFFF F040 0024	4	M	Completion of pulse measurement or one-time frequency or period measurement on digital channels 0–31. 1 = pulse or measurement complete 0 = incomplete or not applicable
FFFF F040 0100	100	UI	Counter data (unsigned integer)

Last valid address for this area: FFFF F040 01FF

DIGITAL BANK WRITE—READ/WRITE

PAC-R
EB
SB
UIO
EIO
SIO
E1
G4EB2

NOTE: To clear counters and latches, use the "Digital Read and Clear" area on page 136.

Applies to most digital modules. (Does not apply to *groov* I/O units, *groov* RIO modules, or SNAP high-density digital modules; see "High-Density Digital Write—Read/Write" on page 148.)

Although this area is read/write, you would normally write to it. For help in formatting data, see "Mask Data" on page 58. For general information on using counters, see page 33.

Starting Address	Length (hex)	Type	Description
FFFF F050 0000	8	M	Turn on (mask)
FFFF F050 0008	8	M	Turn off (mask)
FFFF F050 0010	8	M	Activate counters (mask)
FFFF F050 0018	8	M	Deactivate counters (mask)

Last valid address for this area: FFFF F050 001F

ANALOG BANK READ—READ ONLY

PAC-R
EB
SB
UIO
EIO
SIO
E2

For help in interpreting data, see "IEEE Float Data" on page 61. (Does not apply to *groov* I/O units or *groov* RIO modules.)

Starting Address	Length (hex)	Type	Description
FFFF F060 0000	100	F	Analog data (float—Engineering Units)
FFFF F060 0100	100	F	Analog data (float—counts)
FFFF F060 0200	100	F	Analog Min Value (float—Engineering Units)
FFFF F060 0300	100	F	Analog Max Value (float—Engineering Units)

Last valid address for this area: FFFF F060 03FF

ANALOG BANK WRITE—READ/WRITE

PAC-R
EB
SB
UIO
EIO
SIO
E2

(Does not apply to *groov* I/O units or *groov* RIO modules.) Although this area is read/write, you would normally write to it. For help in formatting data, see "IEEE Float Data" on page 61.

If you're using SNAP firmware version R9.4d or higher, if you write an invalid floating channel value (called a NaN), the invalid float is not written to the analog channel. This way multiple masters can write to the analog bank area and not invalidate values other masters are controlling.

A NaN is a 32-bit value that has 1s in the following binary number locations:
`x111 1111 1xxx xxxx xxxx xxxx xxxx xxxx`

Here is a link to more information on the IEEE-754 definition of a NaN.

Starting Address	Length (hex)	Type	Description
FFFF F070 0000	100	F	Analog output (float—Engineering Units)
FFFF F070 0100	100	F	Analog output (float—counts)

Last valid address for this area: FFFF F070 01FF

DIGITAL CHANNEL READ—READ ONLY

PAC-R
EB
SB
UIO
EIO
SIO
E1
G4EB2

***NOTE**: To clear counters and latches, use the "Digital Read and Clear" area on page 136.*

Applies to most digital modules. (Does not apply to *groov* I/O units, *groov* RIO modules, or SNAP high-density digital modules; instead, see "High-Density Digital—Read Only" on page 147.) For E1 brains, read the first channel of each module.

See "Digital Channel Data (4-Channel Modules)" on page 60 for help in interpreting data. For information on using counters, see page 33. Only the first three channels are shown in the table. Each successive channel starts on an even 40 hex boundary and follows the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F080 0000	4	B	Module 0, Channel 0 (0,0): Channel state. This address is read/write. Read the channel state at this address or write to it: 0 = turn channel off; non-0 = turn channel on
FFFF F080 0004	4	B	0,0: On-latch state. 0 = off; non-0 = on
FFFF F080 0008	4	B	0,0: Off-latch state. 0 = off; non-0 = on
FFFF F080 000C	4	B	0,0: Counter active? 0 = off; non-0 = on
FFFF F080 0010	4	UI	0,0: Feature value (counter, pulse measurement, frequency or period measurement). Units and resolution are in increments of 100 microsecond. Max value is 4,294,967,295. When it reaches max, the value rolls over to zero and continues.
FFFF F080 0040	4	B	0,1: Channel state. This address is read/write. Read the channel state at this address or write to it: 0 = turn channel off; non-0 = turn channel on
FFFF F080 0044	4	B	0,1: On-latch state. 0 = off; non-0 = on
FFFF F080 0048	4	B	0,1: Off-latch state. 0 = off; non-0 = on
FFFF F080 004C	4	B	0,1: Counter active? 0 = off; non-0 = on
FFFF F080 0050	4	UI	0,1: Feature value (counter, pulse measurement, frequency or period measurement). Max value is 4,294,967,295. When it reaches max, the value rolls over to zero and continues
FFFF F080 0080	4	B	0, 2: Channel state. This address is read/write. Read the channel state at this address or write to it: 1 = turn channel on; 0 = turn channel off.

Starting Address	Length (hex)	Type	Description
FFFF F080 0084	4	B	0,2: On-latch state. 0 = off; non-0 = on
FFFF F080 0088	4	B	0,2: Off-latch state. 0 = off; non-0 = on
FFFF F080 008C	4	B	0,2: Counter active? 0 = off; non-0 = on
FFFF F080 0090	4	UI	0,2: Feature value (counter, pulse measurement, frequency or period measurement). Units and resolution are in increments of 100 microseconds. Max value is 4,294,967,295. When it reaches max, the value rolls over to zero and continues
Additional channels follow in order on even 40 hex boundaries.			
FFFF F080 0FC0	4	B	15,3: Channel state. This address is read/write. Read the channel state at this address or write to it: 0 = turn channel off; non-0 = turn channel on

Last valid address for this area: FFFF F080 0FD3

DIGITAL CHANNEL WRITE—READ/WRITE

PAC-R
EB
SB
UIO
EIO
SIO
E1
G4EB2

Applies to most digital modules. (Does not apply to *groov* I/O units, *groov* RIO modules, or SNAP high-density digital modules; instead, see "High-Density Digital Write—Read/Write" on page 148.) For E1 brains, write to the first channel (channel 0) of each module.

Although this area is read/write, you would normally write to it. See "Digital Channel Data (4-Channel Modules)" on page 60 for help in formatting data. For information on using counters, see page 33.

NOTE: To turn channels on and off, you can also write to the channel state address in the Digital Channel Read area (page 121).

Only the first three channels are shown in the table. Each successive channel starts on an even 40 hex boundary and follows the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F090 0000	4	B	Module 0, Channel 0 (0,0): Turn on (Boolean) 0 = no effect; non-0 = turn on channel
FFFF F090 0004	4	B	0,0: Turn off (Boolean) 0 = no effect; non-0 = turn off channel
FFFF F090 0008	4	B	0,0: Activate counter (Boolean) 0 = no effect; non-0 = activate
FFFF F090 000C	4	B	0,0: Deactivate counter (Boolean) 0 = no effect; non-0 = deactivate
FFFF F090 0040	4	B	0,1: Turn on (Boolean) 0 = no effect; non-0 = turn on channel
FFFF F090 0044	4	B	0,1: Turn off (Boolean) 0 = no effect; non-0 = turn off channel
FFFF F090 0048	4	B	0,1: Activate counter (Boolean) 0 = no effect; non-0 = activate
FFFF F090 004C	4	B	0,1: Deactivate counter (Boolean) 0 = no effect; non-0 = deactivate
FFFF F090 0080	4	B	0,2: Turn on (Boolean) 0 = no effect; non-0 = turn on channel
FFFF F090 0084	4	B	0,2: Turn off (Boolean) 0 = no effect; non-0 = turn off channel
FFFF F090 0088	4	B	0,2: Activate counter (Boolean) 0 = no effect; non-0 = activate
FFFF F090 008C	4	B	0,2: Deactivate counter (Boolean) 0 = no effect; non-0 = deactivate
Additional channels follow in order on even 40 hex boundaries.			
FFFF F090 0FC0	4	B	15,3: Turn on (Boolean) 0 = no effect; non-0 = turn on channel

Last valid address for this area: FFFF F090 0FCF

(OLD) ANALOG CHANNEL READ—READ ONLY

UIO
EIO
SIO
E2

Use this section only for E2 I/O units and for SNAP I/O units with firmware versions 7.1 or lower. For SNAP I/O units with firmware version R8.0 or higher, see page 88.

See "IEEE Float Data" on page 61 for help in interpreting data. For E2s, read the first channel (channel 0) on each module.

Only the first three channels are shown in the table. Each successive channel starts on an even 40 hex boundary and follows the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F0A0 0000	4	F	Module 0, Channel 0 (0,0): Analog input/output data (float—Engineering Units)
FFFF F0A0 0004	4	F	0,0: Analog input/output data (float—counts)
FFFF F0A0 0008	4	F	0,0: Analog Min Value (float—Engineering Units)
FFFF F0A0 000C	4	F	0,0: Analog Max Value (float—Engineering Units)
FFFF F0A0 0010	4	–	Reserved
FFFF F0A0 0040	4	F	0,1: Analog input/output data (float—Engineering Units)
FFFF F0A0 0044	4	F	0,1: Analog input/output data (float—counts)
FFFF F0A0 0048	4	F	0,1: Analog Min Value (float—Engineering Units)
FFFF F0A0 004C	4	F	0,1: Analog Max Value (float—Engineering Units)
FFFF F0A0 0080	4	F	0,2: Analog input/output data (float—Engineering Units)
FFFF F0A0 0084	4	F	0,2: Analog input/output data (float—counts)
FFFF F0A0 0088	4	F	0,2: Analog Min Value (float—Engineering Units)
FFFF F0A0 008C	4	F	0,2: Analog Max Value (float—Engineering Units)
Additional channels follow in order on even 40 hex boundaries.			
FFFF F0A0 0FC0	4	F	15,3: Analog input/output data (float—Engineering Units)

Last valid address for this area: FFFF F0A0 0FCF

(OLD) ANALOG CHANNEL WRITE—READ/WRITE

UIO
EIO
SIO
E2

Use this section only for E2 I/O units and for SNAP I/O units with firmware versions 7.1 or lower. For SNAP I/O units with firmware version R8.0 or higher, see page 89.

Although this area is read/write, you would normally write to it. See "IEEE Float Data" on page 61 for help in formatting data. For E2s, write to the first channel (channel 0) on each module.

Only the first three channels are shown in the table. Each successive channel starts on an even 40 hex boundary and follows the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F0B0 0000	4	F	Module 0, Channel 0 (0,0): Output analog data (float—Engineering Units)
FFFF F0B0 0004	4	F	0,0: Output analog data (float—counts)
FFFF F0B0 0008	4	F	0,0: TPO resolution
FFFF F0B0 000C	4	F	0,0: TPO period (float—units of time in seconds. Valid range: 0.25 to 64.0 seconds, in 0.25 steps.) (Not for E2s.)
FFFF F0B0 0010	4	–	0,0: Reserved

Starting Address	Length (hex)	Type	Description
FFFF F0B0 0014	4	UI	0,0: Load cell fast settle level—For SNAP-AILC modules only. (Not for E2s.) Use with load cell filter weight (next address) to get filtered readings faster. Valid values: 0–32,767. 0 = disabled;
FFFF F0B0 0018	4	UI	0,0: Load cell filter weight—For SNAP-AILC modules only. (Not for E2s.) Valid values: 0–255; default = 128. A larger value increases filtering. Use with F0B00014 to get the filtered reading faster. Note that 0, 1, or 255 value disables fast settle level (F0B00014). The second channel on the module is the filtered reading of the first channel.
FFFF F0B0 0040	4	F	0,1: Output analog data (float—Engineering Units)
FFFF F0B0 0044	4	F	0,1: Output analog data (float—counts)
FFFF F0B0 004C	4	F	0,1: TPO period (float—units of time in seconds. Valid range: 0.25 to 64.0 seconds, in 0.25 steps.) (Not for E2s.)
FFFF F0B0 0080	4	F	0,2: Output analog data (float—Engineering Units)
FFFF F0B0 0084	4	F	0,2: Output analog data (float—counts)
FFFF F0B0 008C	4	F	0,2: TPO period (float—units of time in seconds. Valid range: 0.25 to 64.0 seconds, in 0.25 steps.) (Not for E2s.)
Additional channels follow in order on even 40 hex boundaries.			
FFFF F0B0 0FC0	4	F	15,3: Output analog data (float—Engineering Units)
Last valid address for this area: FFFF F0B0 0FCF			

(OLD) ANALOG AND DIGITAL CHANNEL CONFIGURATION INFORMATION—READ/WRITE

UIO
EIO
SIO
E1
E2

Use this section only for E1 and E2 I/O units and for SNAP I/O units with firmware versions 7.1 or lower. For SNAP I/O units with firmware version R8.0 or higher, see page 85.

See page 16 for configuration information. This area does not apply to *groov* or SNAP high-density digital modules, which do not require configuration.

Only the first two channels are shown in the table. Each successive channel starts on an even 40 hex boundary and follows the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F0C0 0000	4	UI	Module 0, Channel 0 (0,0): Read only. Module Type (unsigned integer). For SNAP I/O units, module type is the value reported by an analog, serial, or high-density digital module on a SNAP rack. For analog modules on E2 units, the equivalent SNAP module (derived from channel configuration) is returned. Zero is returned for digital modules, no module, or channels that don't exist (for example, the upper two channels on a two-channel analog module). See table on page 127 for values.
FFFF F0C0 0004	4	UI	0,0: Channel Type (unsigned integer). • Use 0x0000 0100 for digital inputs. • Use 0x0000 0180 for digital outputs. • For analog types, see tables starting on page 21.

Starting Address	Length (hex)	Type	Description
FFFF F0C0 0008	4	UI	0,0: Channel Feature (unsigned integer) Digital feature values: • 0x0000 0001 for counter input (configures and starts the counter) • 0x0000 0002 for on-time totalizer input • 0x0000 0003 for period measurement (continuous) • 0x0000 0004 for simple quadrature counter input • 0x0000 0005 for frequency measurement (continuous) • 0x0000 0009 for on-pulse duration measurement (one-time) • 0x0000 000A for off-pulse duration measurement (one-time) • 0x0000 000B for period measurement (one-time) • 0x0000 000C for frequency measurement (one-time) • 0x0000 0012 for off-time totalizer input • 0x0000 0041 quadrature counter input with index. For quadrature counter information, see page 34. Analog feature values: none at present To disable channel features, use 0x0000 0000
FFFF F0C0 000C	4	F	0,0: Analog channel offset (float). Shows 0.0 unless you set an offset value. Brain uses the value you set or a default of 0.0.
FFFF F0C0 0010	4	F	0,0: Analog channel gain (float). Shows 0.0 unless you set a gain value. Brain uses the value you set or a default of 1.0.
FFFF F0C0 0014	4	F	0,0: Channel high scaling factors (float)
FFFF F0C0 0018	4	F	0,0: Channel low scaling factors (float)
FFFF F0C0 001C	4	–	0,0: Reserved
FFFF F0C0 0020	4	F	0,0: Average filter weight (float) (Does not apply to E2.)
FFFF F0C0 0024	4	F	0,0: Watchdog value. EU float for analog and digital. 0 = off, non-0 = on.
FFFF F0C0 0028	4	B	0,0: Enable watchdog (Boolean) 0 = disable; non-0 = enable
FFFF F0C0 002C	4	–	Reserved
FFFF F0C0 0030	10	S-ZT	Channel name
FFFF F0C0 0040	4	UI	0,1: Read only. Module Type (unsigned integer). For SNAP I/O units, module type is the value reported by an analog or special-purpose module on a SNAP rack. For analog modules on E2 units, the equivalent SNAP module (derived from channel configuration) is returned. Zero is returned for digital modules, no module, or channels that don't exist (for example, the upper two channels on a two-channel analog module). See table on page 127 for values.
FFFF F0C0 0044	4	UI	0,1: Channel Type (unsigned integer). • Use 0x0000 0100 for digital inputs. • Use 0x0000 0180 for digital outputs. • For analog types, see tables starting on page 21.

Starting Address	Length (hex)	Type	Description
FFFF F0C0 0048	4	UI	0,1: Channel Feature (unsigned integer) Digital feature values: • 0x0000 0001 for counter input (configures and starts the counter) • 0x0000 0002 for on-time totalizer input • 0x0000 0003 for period measurement (continuous) • 0x0000 0004 for simple quadrature counter input • 0x0000 0005 for frequency measurement (continuous) • 0x0000 0009 for on-pulse duration measurement (one-time) • 0x0000 000A for off-pulse duration measurement (one-time) • 0x0000 000B for period measurement (one-time) • 0x0000 000C for frequency measurement (one-time) • 0x0000 0012 for off-time totalizer input • 0x0000 0041 quadrature counter input with index. For quadrature counter information, see page 34. Analog feature values: none at present To disable channel features, use 0x0000 0000
FFFF F0C0 004C	4	F	0,1: Channel offsets (float)
FFFF F0C0 0050	4	F	0,1: Channel gains (float)
FFFF F0C0 0054	4	F	0,1: Channel high scaling factors (float)
FFFF F0C0 0058	4	F	0,1: Channel low scaling factors (float)
FFFF F0C0 005C	4	–	0,1: Reserved
FFFF F0C0 0060	4	F	0,1: Average filter weight (float)
FFFF F0C0 0064	4	F	0,1: Watchdog value. EU float for analog and digital. 0 = off, non-0 = on.
FFFF F0C0 0068	4	B	0,1: Enable watchdog (Boolean) 0 = disable; non-0 = enable
FFFF F0C0 006C	4	–	Reserved
FFFF F0C0 0070	10	S-ZT	Channel name
Additional channels follow in order on even 40 hex boundaries.			
FFFF F0C0 0FC0	4	UI	15,15: Read only. Module type.
FFFF F0C0 1000	4	F	0,0: Analog output lower clamp (float).
FFFF F0C0 1004	4	F	0,0: Analog output upper clamp (float).
FFFF F0C0 1008	4	F	0,1: Analog output lower clamp (float).
FFFF F0C0 100C	4	F	0,1: Analog output upper clamp (float).
Additional channels follow in order			
FFFF F0C0 11FC	4	F	15,3: Analog output lower clamp (float).
Last valid address for this area: FFFF F0C0 11FF			

(OLD) DIGITAL EVENTS AND REACTIONS—READ/WRITE

PAC-R EB UIO EIO G4EB2

Use this section only for SNAP I/O units with firmware versions R8.0 or lower. For SNAP I/O units with firmware version R8.1 or higher, see page 127.

(Does not apply to SNAP Simple I/O. Does not apply to *groov* or SNAP high-density digital modules.) See page 44 for information on configuring digital events and reactions.

IMPORTANT: *To reduce scanning time, the I/O unit stops scanning digital events when it reaches an unused event. Make sure you use event numbers in order, starting with the lowest.*

Only the first two digital event/reactions are shown in the table. Other event/reactions follow the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F0D0 0000	8	M	Digital event 0: Channels on? (mask)
FFFF F0D0 0008	8	M	Digital event 0: Channels off? (mask)
FFFF F0D0 0010	8	M	Digital reaction 0: Turn channels on (mask)
FFFF F0D0 0018	8	M	Digital reaction 0: Turn channels off (mask)
FFFF F0D0 0020	8	M	Digital event 0: Scratch Pad bits on? (mask)
FFFF F0D0 0028	8	M	Digital event 0: Scratch Pad bits off? (mask)
FFFF F0D0 0030	8	M	Digital reaction 0: Turn Scratch Pad bits on (mask)
FFFF F0D0 0038	8	M	Digital reaction 0: Turn Scratch Pad bits off (mask)
FFFF F0D0 0040	8	M	Digital event 1: Channels on? (mask)
FFFF F0D0 0048	8	M	Digital event 1: Channels off? (mask)
FFFF F0D0 0050	8	M	Digital reaction 1: Turn channels on (mask)
FFFF F0D0 0058	8	M	Digital reaction 1: Turn channels off (mask)
FFFF F0D0 0060	8	M	Digital event 1: Scratch Pad bits on? (mask)
FFFF F0D0 0068	8	M	Digital event 1: Scratch Pad bits off? (mask)
FFFF F0D0 0060	8	M	Digital reaction 1: Turn Scratch Pad bits on (mask)
FFFF F0D0 0068	8	M	Digital reaction 1: Turn Scratch Pad bits off (mask)

Other digital event/reactions follow in order on even 40 hex boundaries.

Last valid address for this area: FFFF F0D0 1FFF

DIGITAL EVENTS - EXPANDED (FORMERLY TIMERS)—READ/WRITE

PAC-R EB SB G4EB2

For SNAP I/O units with firmware versions R8.1 and higher, use this section for all digital event configuration. See addresses below. (Does not apply to *groov* I/O units or *groov* RIO modules.)

For SNAP I/O units with firmware versions R8.0 and lower, this section provides Timer configuration only, with limited options. See addresses on page 132.

For event capabilities of devices and firmware versions, see the charts starting on page 40.

Addresses for SNAP Firmware R8.1 and Higher

IMPORTANT: *To reduce scanning time, the I/O unit stops scanning digital events when it reaches an unused event. Make sure you use event numbers in order, starting with the lowest.*

Only the first two digital events are shown in the table. Others follow the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F0D4 0000	8	M	Event 0: Trigger #1 ON mask that triggers the event (details of event trigger are determined by the mask in F0D4 0044)
FFFF F0D4 0008	8	M	Event 0: Trigger #1 OFF mask that triggers the event
FFFF F0D4 0010	8	M	Event 0: Trigger #2 ON mask that triggers the event
FFFF F0D4 0018	8	M	Event 0: Trigger #2 OFF mask that triggers the event
FFFF F0D4 0020	8	M	Event 0: Trigger #1 ON mask to be set as a reaction to the event
FFFF F0D4 0028	8	M	Event 0: Trigger #1 OFF mask to be set as a reaction to the event
FFFF F0D4 0030	8	M	Event 0: Trigger #2 ON mask to be set as a reaction to the event
FFFF F0D4 0038	8	M	Event 0: Trigger #2 OFF mask to be set as a reaction to the event
FFFF F0D4 0040	4	UI	Event 0: Time between event and reaction, in milliseconds

<table>
<tr><th>Starting Address</th><th>Length (hex)</th><th>Type</th><th>Description</th></tr>
<tr><td>FFFF F0D4 0044</td><td>4</td><td>M</td><td>Event 0: Event detail mask, specifying triggers and reactions. For examples, see “Event Detail Mask” on page 46.
<table>
<tr><th>Bit</th><th>Purpose</th></tr>
<tr><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>Trigger 1—Latches = 1; digital channel state = 0</td></tr>
<tr><td>2</td><td>If bit 1 is set (latches)—On-latches = 1; off-latches = 0</td></tr>
<tr><td>3</td><td>Reaction 1—Clear on- and off-latches = 1; states = 0</td></tr>
<tr><td>4</td><td>Trigger 1—Use HDD module specified in F0D4 0050 = 1; use 4-ch digital module = 0</td></tr>
<tr><td>5</td><td>Reaction 1—Use HDD module specified in F0D4 0054 = 1; use 4-ch digital module = 0</td></tr>
<tr><td>6</td><td>Trigger 2—Use Scratch Pad Integer 64 specified in F0D4 0058 = 1; use Scratch Pad Bit = 0</td></tr>
<tr><td>7</td><td>Reaction 2—Use Scratch Pad Integer 64 specified in F0D4 005C = 1; use Scratch Pad Bit = 0</td></tr>
<tr><td>8</td><td>Reaction—Send reaction only once = 1; send reaction continuously, as long as the event is still occurring = 0</td></tr>
<tr><td>9–14</td><td>Reserved</td></tr>
<tr><td>15</td><td>Trigger 1 Source—Scratch Pad, defined in bit 24 = 1; digital, defined in bit 4 = 0</td></tr>
<tr><td>16</td><td>Trigger 2 Source—Digital, defined in bit 22 = 1; Scratch Pad, defined in bit 6 = 0</td></tr>
<tr><td>17</td><td>Trigger 2—If bit 16 is set, digital channel latch = 1; digital channel state = 0</td></tr>
<tr><td>18</td><td>Trigger 2—If bits 16 and 17 are set, on-latch = 1; off-latch = 0</td></tr>
<tr><td>19</td><td>Reaction 2—Clear latches = 1; states = 0</td></tr>
<tr><td>20</td><td>Reaction 1 Source—Scratch Pad, defined in 25 = 1; digital, defined in bit 5 = 0</td></tr>
<tr><td>21</td><td>Reaction 2 Source—Digital, defined in bit 23 = 1; Scratch Pad, defined in bit 7 = 0</td></tr>
<tr><td>22</td><td>Trigger 2—Use HDD module specified in F0D4 0050 = 1; use 4-ch digital module = 0</td></tr>
<tr><td>23</td><td>Reaction 2—Use HDD module specified in F0D4 0054 = 1; use 4-ch digital module = 0</td></tr>
<tr><td>24</td><td>Trigger 1—Use Scratch Pad Integer 64 specified in F0D4 0058 = 1; use Scratch Pad Bit = 0</td></tr>
</table></td></tr>
</table>

Starting Address	Length (hex)	Type	Description
FFFF F0D4 0048	4	UI	Event 0: Time remaining until the reaction, in milliseconds
FFFF F0D4 004C	4	UI	Event 0: Event state: 0 = event is enabled but not occurring now 1 = event is occurring 2 = event has occurred and reaction has not been sent (in delay period) 3 = event has occurred and reaction has been sent (applies only if bit 8 in F0D4 0044 is set to send the reaction just once) 4 = event is disabled
FFFF F0D4 0050	4	UI	Event 0: HDD module number to use for digital event trigger #1
FFFF F0D4 0054	4	UI	Event 0: HDD module number to use for digital reaction #1
FFFF F0D4 0058	4	UI	Event 0: Scratch Pad Integer 64 index to use for digital event trigger #2
FFFF F0D4 005C	4	UI	Event 0: Scratch Pad Integer 64 index to use for digital event reaction #2
FFFF F0D4 0060	20	–	Reserved
FFFF F0D4 0080	8	M	Event 1: Trigger #1 ON mask that triggers the event (details of event trigger are determined by the mask in F0D4 0044)
FFFF F0D4 0088	8	M	Event 1: Trigger #1 OFF mask that triggers the event
FFFF F0D4 0090	8	M	Event 1: Trigger #2 ON mask that triggers the event
FFFF F0D4 0098	8	M	Event 1: Trigger #2 OFF mask that triggers the event
FFFF F0D4 00A0	8	M	Event 1: Trigger #1 ON mask to be set as a reaction to the event
FFFF F0D4 00A8	8	M	Event 1: Trigger #1 OFF mask to be set as a reaction to the event
FFFF F0D4 00B0	8	M	Event 1: Trigger #2 ON mask to be set as a reaction to the event
FFFF F0D4 00B8	8	M	Event 1: Trigger #2 OFF mask to be set as a reaction to the event
FFFF F0D4 00C0	4	UI	Event 1: Time between event and reaction, in milliseconds

<table>
<tr><th>Starting Address</th><th>Length (hex)</th><th>Type</th><th>Description</th></tr>
<tr><td>FFFF F0D4 00C4</td><td>4</td><td>M</td><td>Event 1: Event detail mask, specifying triggers and reactions. For examples, see “Event Detail Mask” on page 46.
<table>
<tr><th>Bit</th><th>Purpose</th></tr>
<tr><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>Trigger 1—Latches = 1; digital channel state = 0</td></tr>
<tr><td>2</td><td>If bit 1 is set (latches)—On-latches = 1; off-latches = 0</td></tr>
<tr><td>3</td><td>Reaction 1—Clear on- and off-latches = 1; states = 0</td></tr>
<tr><td>4</td><td>Trigger 1—Use HDD module specified in F0D4 00D0 = 1; use 4-ch digital module = 0</td></tr>
<tr><td>5</td><td>Reaction 1—Use HDD module specified in F0D4 00D4 = 1; use 4-ch digital module = 0</td></tr>
<tr><td>6</td><td>Trigger 2—Use Scratch Pad Integer 64 specified in F0D4 00D8 = 1; use Scratch Pad Bit = 0</td></tr>
<tr><td>7</td><td>Reaction 2—Use Scratch Pad Integer 64 specified in F0D4 00DC = 1; use Scratch Pad Bit = 0</td></tr>
<tr><td>8</td><td>Reaction—Send reaction only once = 1; send reaction continuously, as long as the event is still occurring = 0</td></tr>
<tr><td>9–14</td><td>Reserved</td></tr>
<tr><td>15</td><td>Trigger 1 Source—Scratch Pad, defined in bit 24 = 1; digital, defined in bit 4 = 0</td></tr>
<tr><td>16</td><td>Trigger 2 Source—Digital, defined in bit 22 = 1; Scratch Pad, defined in bit 6 = 0</td></tr>
<tr><td>17</td><td>Trigger 2—If bit 16 is set, digital channel latch = 1; digital channel state = 0</td></tr>
<tr><td>18</td><td>Trigger 2—If bits 16 and 17 are set, on-latch = 1; off-latch = 0</td></tr>
<tr><td>19</td><td>Reaction 2—Clear latches = 1; states = 0</td></tr>
<tr><td>20</td><td>Reaction 1 Source—Scratch Pad, defined in 25 = 1; digital, defined in bit 5 = 0</td></tr>
<tr><td>21</td><td>Reaction 2 Source—Digital, defined in bit 23 = 1; Scratch Pad, defined in bit 7 = 0</td></tr>
<tr><td>22</td><td>Trigger 2—Use HDD module specified in F0D4 00D0 = 1; use 4-ch digital module = 0</td></tr>
<tr><td>23</td><td>Reaction 2—Use HDD module specified in F0D4 00D4 = 1; use 4-ch digital module = 0</td></tr>
<tr><td>24</td><td>Trigger 1—Use Scratch Pad Integer 64 specified in F0D4 00D8 = 1; use Scratch Pad Bit = 0</td></tr>
<tr><td>25</td><td>Reaction 1—Use Scratch Pad Integer 64 specified in F0D4 00DC = 1; use Scratch Pad Bit = 0</td></tr>
</table></td></tr>
</table>

Starting Address	Length (hex)	Type	Description
FFFF F0D4 00C8	4	UI	Event 1: Time remaining until the reaction, in milliseconds
FFFF F0D4 00CC	4	UI	Event 1: Event state: 0 = event is enabled but not occurring now 1 = event is occurring 2 = event has occurred and reaction has not been sent (in delay period) 3 = event has occurred and reaction has been sent (applies only if bit 8 in F0D4 00C4 is set to send the reaction just once) 4 = event is disabled
FFFF F0D4 00D0	4	UI	Event 1: HDD module number to use for digital event trigger #1
FFFF F0D4 00D4	4	UI	Event 1: HDD module number to use for digital reaction #1
FFFF F0D4 00D8	4	UI	Event 1: Scratch Pad Integer 64 index to use for digital event trigger #2
FFFF F0D4 00DC	4	UI	Event 1: Scratch Pad Integer 64 index to use for digital event reaction #2
FFFF F0D4 00E0	20	–	Reserved

Other digital events follow in order on even 80 hex boundaries.

Last valid address for this area: FFFF F0D4 FFFF

Addresses for SNAP Firmware R8.0 and Lower

PAC-REB UIO EIO

For SNAP I/O units with firmware versions R8.0 and lower, this section provides only Timer (delay) configuration for digital events. See addresses below. (Does not apply to *groov* I/O units or *groov* RIO modules.)

For SNAP I/O units with firmware versions R8.1 and higher, use this section for all digital event configuration. See addresses on page 127.

For event capabilities of devices and firmware versions, see the charts starting on page 40.

IMPORTANT: *To reduce scanning time, the I/O unit stops scanning digital events when it reaches an unused event. Make sure you use event numbers in order, starting with the lowest.*

Only the first two timer events are shown in the table. Others follow the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F0D4 0000	8	M	Timer 0: Digital ON mask that starts the timer
FFFF F0D4 0008	8	M	Timer 0: Digital OFF mask that starts the timer
FFFF F0D4 0010	8	M	Timer 0: Scratch Pad ON mask that starts the timer
FFFF F0D4 0018	8	M	Timer 0: Scratch Pad OFF mask that starts the timer
FFFF F0D4 0020	8	M	Timer 0: Digital ON mask to be set when the timer expires
FFFF F0D4 0028	8	M	Timer 0: Digital OFF mask to be set when the timer expires
FFFF F0D4 0030	8	M	Timer 0: Scratch Pad ON mask to be set when the timer expires
FFFF F0D4 0038	8	M	Timer 0: Scratch Pad OFF mask to be set when the timer expires
FFFF F0D4 0040	4	UI	Timer 0: Length of the timer delay, in milliseconds
FFFF F0D4 0044	4	–	Reserved
FFFF F0D4 0048	4	UI	Timer 0: Time remaining until the timer expires, in milliseconds
FFFF F0D4 004C	4	UI	Timer 0: Timer state. 0 = Timer not set; 1 = Timer set; 2 = Timer is ticking
FFFF F0D4 0050	30	–	Pad for alignment

Starting Address	Length (hex)	Type	Description
FFFF F0D4 0080	8	M	Timer 1: Digital ON mask that starts the timer
FFFF F0D4 0088	8	M	Timer 1: Digital OFF mask that starts the timer
FFFF F0D4 0090	8	M	Timer 1: Scratch Pad ON mask that starts the timer
FFFF F0D4 0098	8	M	Timer 1: Scratch Pad OFF mask that starts the timer
FFFF F0D4 00A0	8	M	Timer 1: Digital ON mask to be set when the timer expires
FFFF F0D4 00A8	8	M	Timer 1: Digital OFF mask to be set when the timer expires
FFFF F0D4 00B0	8	M	Timer 1: Scratch Pad ON mask to be set when the timer expires
FFFF F0D4 00B8	8	M	Timer 1: Scratch Pad OFF mask to be set when the timer expires
FFFF F0D4 00C0	8	UI	Timer 1: Length of the timer delay, in milliseconds
FFFF F0D4 00C4	4	–	Reserved
FFFF F0D4 00C8	4	UI	Timer 1: Time remaining until the timer expires, in milliseconds
FFFF F0D4 00CC	8	UI	Timer 1: Timer state. 0 = Timer not set; 1 = Timer set; 2 = Timer is ticking
FFFF F0D4 00D0	30	–	Pad for alignment

Other timers follow in order on even 80 hex boundaries.

Last valid address for this area: FFFF F0D4 FFFF

CUSTOM CONFIGURATION AREA—WRITE

Use this area to configure a custom series of memory map addresses you want to read or write to in one operation. For example, you can use this area to configure custom streaming (see page 53) or create a block read or write of various memory map addresses.

Use the Custom Data Access area (page 134) to read and write the data you've configured.

Starting Address	Length (hex)	Type	Description
FFFF F0D5 0000	4	UI	Element 0: First memory map address for custom area
FFFF F0D5 0004	4	UI	Element 1: Next memory map address for custom area
FFFF F0D5 0008	4	UI	Element 2: Next memory map address for custom area
Additional elements follow in order on even 4 hex boundaries. Total at this address: 1024			
FFFF F0D5 0FFC	4	UI	Element 1023: Last memory map address for custom area

Last valid address for this area: FFFF F0D5 0FFF

* Data type is determined by the addresses you enter.

CUSTOM DATA ACCESS AREA—READ/WRITE

Use this area in conjunction with the Custom Configuration area (page 133) to read or write to a preconfigured set of memory map addresses in one operation. For example, you can use this area to stream non-contiguous addresses (see page 53).

If you access an address in this area that does not have an associated address specified in the Custom Configuration area, reads will always return 0, and writes will have no effect.

This area must be accessed only on 4-byte boundaries, in lengths that are integer multiples of 4. For example, you can access F0D60004 with a length of 8, but not F0D60005 with a length of 3.

Starting Address	Length (hex)	Type	Description
FFFF F0D6 0000	4	*	Element 0: Reads or writes to the memory map address in F0D50000
FFFF F0D6 0004	4	*	Element 1: Reads or writes to the memory map address in F0D50004
FFFF F0D6 0008	4	*	Element 2: Reads or writes to the memory map address in F0D50008
Additional elements follow in order on even 4 hex boundaries. Total at this address: 1024			
FFFF F0D6 0FFC	4	*	Element 1023: Reads or writes to the memory map address in F0D50FFC

Last valid address for this area: FFFF F0D6 0FFF

* Data type is determined by the addresses you configured in the Custom Configuration Area (page 133).

SCRATCH PAD—READ/WRITE

PR1
RIO
PAC-R
PAC-S
EB
SB
UIO
EIO
LCE
G4EB2

For EIO units, only Scratch Pad bits apply. For other devices, the Scratch Pad area is used to share data among devices on the network. Since each Scratch Pad read or write operation is atomic, reads and writes will not interfere with each other.

Scratch Pad 64-Bit Integers apply only to *groov* I/O units, *groov* RIO modules, and SNAP I/O units with firmware version R8.1 and higher. For more information on using the Scratch Pad area, see page 38.

This area is stored to flash only on manual saves.

NOTE: Scratch Pad strings can be null terminated or can be binary strings with embedded nulls. Length is automatically calculated, but can be written to force a specific length. If the length and the string are written together, the length written is used.

Starting Address	Length (hex)	Type	Description
FFFF F0D8 0000	8	M	Current state of Scratch Pad bits (mask). 1 = bit on; 0 = bit off.
FFFF F0D8 0400	8	M	Set Scratch Pad On mask. 1 = set bit on; 0 = no change.
FFFF F0D8 0408	8	M	Set Scratch Pad Off mask 1 = set bit off; 0 = no change.
FFFF F0D8 1000	4	I	Scratch Pad 32-bit Integer element 0.
FFFF F0D8 1004	4	I	Scratch Pad 32-bit Integer element 1.
FFFF F0D8 1008	4	I	Scratch Pad 32-bit Integer element 2.
Additional 32-bit Integer elements follow in order on even 4 hex boundaries. Total at this address: 1024. Additional 9216 starting at address FFFF F0DA 0000			
FFFF F0D8 1FFC	4	I	Scratch Pad 32-bit Integer element 1023.

Starting Address	Length (hex)	Type	Description
FFFF F0D8 2000	4	F	Scratch Pad float element 0.
FFFF F0D8 2004	4	F	Scratch Pad float element 1.
FFFF F0D8 2008	4	F	Scratch Pad float element 2.
Additional float elements follow in order on even 4 hex boundaries. Total at this address: 1024. Additional 9216 starting at address FFFF F0DC 0000			
FFFF F0D8 2FFC	4	F	Scratch Pad float element 1023.
FFFF F0D8 3000	2	UI	Scratch Pad string element 0: Length (integer). If length is not written here, it is automatically calculated by counting to the first null.
FFFF F0D8 3002	80	S-PL	Scratch Pad string element 0: String
FFFF F0D8 3082	2	UI	Scratch Pad string element 1: Length (integer). If length is not written here, it is automatically calculated by counting to the first null.
FFFF F0D8 3084	80	S-PL	Scratch Pad string element 1: String
FFFF F0D8 3104	2	UI	Scratch Pad string element 2: Length (integer). If length is not written here, it is automatically calculated by counting to the first null.
FFFF F0D8 3106	80	S-PL	Scratch Pad string element 2: String
Additional string elements follow in order on even 82 hex boundaries. Total: 64.			
FFFF F0D8 4FFE	2	UI	Scratch Pad string element 63: Length (integer). If length is not written here, it is automatically calculated by counting to the first null.
FFFF F0D8 5000	80	S-PL	Scratch Pad string element 63: String
Last valid address in this section: FFFF F0D8 507F			
FFFF F0DA 0000	4	I	Scratch Pad 32-bit Integer element 1024
FFFF F0DA 0004	4	I	Scratch Pad 32-bit Integer element 1025
FFFF F0DA 0008	4	I	Scratch Pad 32-bit Integer element 1026
Additional 32-bit Integer elements follow in order on even 4 hex boundaries. Total at this address: 9216. Elements 0–1023 start at address FFFF F0D8 1000			
FFFF F0DA 8FFC	4	I	Scratch Pad 32-bit Integer element 10,239
Last valid address in this section: FFFF F0DA 1FFFF			
FFFF F0DC 0000	4	F	Scratch Pad float element 1024
FFFF F0DC 0004	4	F	Scratch Pad float element 1025
FFFF F0DC 0008	4	F	Scratch Pad float element 1026
Additional float elements follow in order on even 4 hex boundaries. Total at this address: 9216. Elements 0–1023 start at address FFFF F0D8 2000			
FFFF F0DC 8FFC	4	F	Scratch Pad float element 10,239
Last valid address in this section: FFFF F0DC 8FFF			
FFFF F0DE 0000	8	M	Scratch Pad 64-bit Integer element 0
FFFF F0DE 0008	8	M	Scratch Pad 64-bit Integer element 1
FFFF F0DE 0010	8	M	Scratch Pad 64-bit Integer element 2
Additional 64-bit Integer elements follow in order on even 8 hex boundaries. Total at this address: 1024			
FFFF F0DE 1FF8	8	M	Scratch Pad 64-bit Integer element 1023
Last valid address in this section: FFFF F0DE 1FFF			
Last valid address for this area: FFFF F0DC 81FF			

(OLD) ANALOG CHANNEL CALCULATION AND SET—READ ONLY

UIO
EIO
SIO
E2

Use this section only for E2 I/O units and for SNAP I/O units I/O units with firmware versions 7.1 or lower. For SNAP I/O units with firmware version R8.0 or higher, see page 87.

When you read data in this area, the data is returned and set.

CAUTION: *Reading any portion of a quadlet (for example, the first byte of a four-byte quadlet) sets the offset or gain but returns only the one-byte value requested, which is incomplete.*

Offset assumes that zero-scale counts are on the input. Gain assumes that full-scale counts are on the input. Offset and gain are typically used for calibration, and offset should be done before gain.

Only the first four channels are shown. Each successive channel starts on an even 4 hex boundary and follows the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F0E0 0000	4	F	Module 0, Channel 0 (0,0): Offset in Engineering Units (float)
FFFF F0E0 0004	4	F	0,1: Offset in Engineering Units (float)
FFFF F0E0 0008	4	F	0,2: Offset in Engineering Units (float)
FFFF F0E0 000C	4	F	Channel 3: Offset in Engineering Units (float)
Additional channels follow in order on even 4 hex boundaries.			
FFFF F0E0 00FC	4	F	15,15 Offset in Engineering Units (float)
FFFF F0E0 0100	4	F	0,0: Gain (float)
FFFF F0E0 0104	4	F	0,1: Gain (float)
FFFF F0E0 0108	4	F	0,2: Gain (float)
FFFF F0E0 010C	4	F	Channel 3: Gain (float)
Additional channels follow in order on even 4 hex boundaries.			
FFFF F0E0 01FC	4	F	15,15 Gain (float)
Last valid address for this area: FFFF F0E0 01FF			

(OLD) DIGITAL READ AND CLEAR—READ ONLY

UIO
EIO
SIO
E1

Use this section only for E1 I/O units and for SNAP I/O units with firmware versions 7.1 or lower. For SNAP I/O units with firmware version R8.0 or higher, see page 90. Do not use this section for *groov* or SNAP high-density digital channels; see "High-Density Digital Read and Clear—Read/Write" on page 147.

When you read data from this area, the data is returned and then cleared.

Only the first two channels are shown. Each successive channel starts on an even 4 hex boundary and follows the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F0F0 0000	4	UI	Module 0, Channel 0 (0,0): Counts (unsigned integer)
FFFF F0F0 0004	4	UI	0,1: Counts (unsigned integer)
Additional channels follow in order on even 4 hex boundaries.			
FFFF F0F0 00FC	4	UI	15,3: Counts (unsigned integer)
FFFF F0F0 0100	4	B	0,0: On-Latch (Boolean) 0 = off; non-0 = on
FFFF F0F0 0104	4	B	0,1: On-Latch (Boolean) 0 = off; non-0 = on

Starting Address	Length (hex)	Type	Description
Additional channels follow in order on even 4 hex boundaries.			
FFFF F0F0 01FC	4	B	15,3: On-Latch (Boolean) 0 = off; non-0 = on
FFFF F0F0 0200	4	B	0,0: Off-Latch (Boolean) 0 = off; non-0 = on
FFFF F0F0 0204	4	B	0,1: Off-Latch (Boolean) 0 = off; non-0 = on
Additional channels follow in order on even 4 hex boundaries.			
FFFF F0F0 02FC	4	B	15,3: Off-Latch (Boolean) 0 = off; non-0 = on
Last valid address for this area: FFFF F0F0 02FF			

(OLD) ANALOG READ AND CLEAR/RESTART—READ ONLY

UIO
EIO
SIO
E2

Use this section only for E2 I/O units and for SNAP I/O units with firmware versions 7.1 or lower. For SNAP I/O units with firmware version R8.0 or higher, see page 87.

When you read data from this area, the data is returned and then cleared or reset.

*NOTE: This area returns a **NaN** for any analog or digital feature with a bad quality reading and for unused[2] I/O module positions. It also returns a NaN for unused points on PAC-R, EB, SB, E2, and GBEB2 devices. If the device being read is a **groov EPIC PR1**, see KB87680.*

***CAUTION:** If you read or write less than a quadlet in this area of the memory map, the returned data will be useless and the information will be erased (cleared).*

Only the first two channels are shown. Each successive channel starts on an even 4 hex boundary and follows the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F0F8 0000	4	F	Module 0, Channel 0 (0,0): Min Data (float)
FFFF F0F8 0004	4	F	0,1: Min Data (float)
Additional channels follow in order on even 4 hex boundaries.			
FFFF F0F8 00FC	4	F	15,3: Min Data (float)
FFFF F0F8 0100	4	F	0,0: Max Data (float)
FFFF F0F8 0104	4	F	0,1: Max Data (float)
Additional channels follow in order on even 4 hex boundaries.			
FFFF F0F8 01FC	4	F	15,3: Max Data (float)
Last valid address for this area: FFFF F0F8 01FF			

[2] An unused I/O module position is a module position that doesn't have an analog module, or it has a digital module without features (for example, a counter) configured.
Similarly, a channel address is "unused" when:
- The number of address spaces reserved for channels in the memory map is greater than the number of channels present. For example, if the memory map has room for 32 channels but the I/O module has only 2 channels, 2 addresses will report values and the 30 unused addresses will report a NaN.
- (PAC-R, EB, SB, E2, and G4EB2) An analog channel is not configured.
- (Digital channels only) A digital channel doesn't have a feature or its feature isn't configured.

For more information, see KB87680, On a PR1, unused analog and digital feature channels return 0.0 instead of NaN.

STREAMING—READ ONLY

PR1
RIO
PAC-R
EB
UIO
EIO
SIO
G4EB2

NOTE: The addresses for groov EPIC processors and groov RIO modules are different from those for other devices.

This area can be used in two ways:

- To get this information in a compact form, read this area all at once instead of reading several other sections. (Like the Packed Data areas[3], this area efficiently reads commonly needed data using few transactions.)
- You can stream data from the I/O unit to PCs or other host devices. Streaming sends data at stated intervals automatically and does not require a response. For more information, see "Streaming Data" on page 51.

Addresses for PR1 and RIO

Starting Address	Length (hex)	Type	Description
FFFF F100 0300	800	F/UI	High-density channel data. Can accommodate up to 512 channels (32 channels for each of 16 modules). Analog channels: the value in Engineering Units (float). Digital channels: feature data (unsigned integer). Feature data for each digital channel depends on channel configuration. Note that *groov* "simple" I/O modules support only the *state* digital feature; for details, see "Selecting Configuration Values for I/O Channel Features" on page 31.
FFFF F100 0B00	40	M	Digital channel state. 0 = Off; 1 = On. Up to 32 channels on 16 modules.
FFFF F100 0B40	40	M	Digital channel on-latches. 0 = Off; 1 = On. Up to 32 channels on 16 modules.
FFFF F100 0B80	40	M	Digital channel off-latches. 0 = Off; 1 = On. Up to 32 channels on 16 modules.
FFFF F100 0BC0	40	M	Channel present. Indicates whether a channel is present in the specified location. Present = 1; not present = 0. Up to 32 channels on 16 modules.

Last valid address for this area: FFFF F100 0BFF

Addresses for PAC-R, EB, UIO, EIO, SIO, and G4EB2 Devices

Starting Address	Length (hex)	Type	Description
FFFF F100 0000	100	F	Analog Engineering Units data for 64 channels (float). Includes the first four channels on 16 analog modules; if an analog module has more than four channels, data is included for channels 0-3 only.
FFFF F100 0100	100	UI	Digital channel feature data (unsigned integer). Feature data for each channel depends upon the channel configuration.
FFFF F100 0200	8	M	State of 4-channel digital channels. (Does not include high-density digital channels.) 0 = Off; 1 = On.
FFFF F100 0208	8	M	Digital on-latches. (Does not include high-density digital channels.) 0 = Off; 1 = On.
FFFF F100 0210	8	M	Digital off-latches. (Does not include high-density digital channels.) 0 = Off; 1 = On.
FFFF F100 0218	8	M	Active counters (mask).

Last valid address for this area: FFFF F100 021F

[3] *Packed Data* areas put large amounts of related data into one area of the memory map so it's faster and easier to read in one transaction.

ANALOG EU OR DIGITAL COUNTER (FEATURE) PACKED DATA—READ

PR1
RIO
PAC-R
EB
SB
E2
G4EB2

This area is for *groov* I/O units, *groov* RIO units, and SNAP I/O units that have firmware version R8.0 and higher. This area has space for 512 channels, the maximum currently available on one I/O unit. Addresses contain either analog Engineering Units (EU) or digital counters, depending on the module installed at that location. Similar to the Digital Packed Data area (see page 139), this area provides an efficient way to read data with the fewest number of transactions.

See "Formatting and Interpreting Data" on page 58 for help in understanding the data you read.

For analog I/O, this area returns a NaN for any bad quality reading and for unused channel addresses[4].

- For a **PAC-R, EB, SB, E2,** or **G4EB2,** the value of the NaN is FF FF FF FF.
- A **PR1** or **RIO** returns 0x7FC00000 for a NaN when representing the first 24 channels of a module. After 24 channels the value reported is 0.

Only the first six channels on the first module are shown in the table. Successive channels and modules follow the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F100 1000	4	F/UI	Module 0, Channel 0 (0,0): If analog channel: value in EU; if digital channel, digital counter value (counter must be configured as channel feature).
FFFF F100 1004	4	F/UI	0,1: Analog channel value or digital counter value
FFFF F100 1008	4	F/UI	0,2: Analog channel value or digital counter value
FFFF F100 100C	4	F/UI	0,3: Analog channel value or digital counter value
FFFF F100 1010	4	F/UI	0,4: Analog channel value or digital counter value
FFFF F100 1014	4	F/UI	0,5: Analog channel value or digital counter value

Additional channels follow in order on 4 hex boundaries.
Additional modules follow in order on 80 hex boundaries.

Last valid address for this area: FFFF F100 17FF

DIGITAL PACKED DATA—READ/WRITE

PR1
RIO
PAC-R
EB
SB
G4EB2

This area is for *groov* I/O units, for *groov* RIO units, and for SNAP I/O units that have firmware version R8.0 and higher. This area has space for 512 channels, the maximum currently available on one I/O unit.

Like the Analog EU or Digital Counter Packed Data area (see previous section) and the Streaming area (see page 138), this area is an efficient way to read or write data with the fewest number of transactions.

The data in this area is masked. If the module has 32 channels, the mask contains the state of all 32 channels, as illustrated below:

At address:	F1001800								→	F1001803							
These bit numbers:	7	6	5	4	3	2	1	0	→	7	6	5	4	3	2	1	0
Show data for these channels:	31	30	29	28	27	26	25	24	→	7	6	5	4	3	2	1	0

[4] A channel address is "unused" when an I/O module has fewer channels than the number of addresses reserved for them in the memory map. For example, if memory addresses have been reserved for 32 channels and the I/O module in that position has only 2 channels, two channel addresses will be used for storing data and the 30 unused addresses will report a NaN.

If the module has 4 channels, the mask contains the following data:

At address:	F1001800	F1001801	F1001802								F1001803							
These bit numbers:	[ignore]	[ignore]	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Show this data:	[zeros—ignore]	[zeros—ignore]	Counter?	Counter?	Counter?	Counter?	Off-latch	Off-latch	Off-latch	Off-latch	On-latch	On-latch	On-latch	On-latch	State	State	State	State
On this channel:	–	–	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0

Only the first four modules are shown in the table. Successive modules follow the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F100 1800	4	M	Module 0. If high-density module, shows states of all channels. If 4-channel module, shows state, whether on-latch and off-latch are set, and whether channel is a configured as a counter.
FFFF F100 1804	4	M	Module 1 (same)
FFFF F100 1808	4	M	Module 2 (same)
FFFF F100 180C	4	M	Module 3 (same)

Last valid address for this area: FFFF F100 183F

ALARM EVENT SETTINGS—READ/WRITE

PAC-R
EB
SB
UIO
EIO

(Does not apply to *groov* I/O units, *groov* RIO modules, or SNAP Simple I/O) Use this area to configure deviation, high limit, and low limit alarm events and reactions. See page 48 for information on configuring alarms and their reactions.

Only the first two alarms are shown in the table. Successive alarms follow the same pattern and start on even 80 hex boundaries.

Starting Address	Length (hex)	Type	Description
FFFF F110 0000	4	B	Alarm 0: Deviation alarm: in alarm state? (Boolean)
FFFF F110 0004	4	B	Alarm 0: Enable deviation alarm (Boolean)
FFFF F110 0008	4	F	Alarm 0: Deviation alarm: previous deviation value (float)
FFFF F110 000C	4	F	Alarm 0: Deviation alarm, deviation amount (float)
FFFF F110 0010	8	M	Alarm 0: Deviation alarm reaction: set Scratch Pad bits on (mask)
FFFF F110 0018	8	M	Alarm 0: Deviation alarm reaction: set Scratch Pad bits off (mask)
FFFF F110 0020	4	B	Alarm 0: High alarm: in alarm state? (Boolean)
FFFF F110 0024	4	B	Alarm 0: Enable high alarm (Boolean)
FFFF F110 0028	4	F	Alarm 0: High alarm setpoint
FFFF F110 002C	4	F	Alarm 0: High alarm deadband
FFFF F110 0030	8	M	Alarm 0: High alarm reaction: set Scratch Pad bits on (mask)
FFFF F110 0038	8	M	Alarm 0: High alarm reaction: set Scratch Pad bits off (mask)
FFFF F110 0040	4	B	Alarm 0: Low alarm: in alarm state? (Boolean)
FFFF F110 0044	4	B	Alarm 0: Enable low alarm (Boolean)
FFFF F110 0048	4	F	Alarm 0: Low alarm setpoint
FFFF F110 004C	4	F	Alarm 0: Low alarm deadband
FFFF F110 0050	8	M	Alarm 0: Low alarm reaction: set Scratch Pad bits on (mask)

Starting Address	Length (hex)	Type	Description
FFFF F110 0058	8	M	Alarm 0: Low alarm reaction: set Scratch Pad bits off (mask)
FFFF F110 0060	4	UI	Alarm 0: Address of value to check. Use to set multiple alarms on one channel. See the *PAC Manager User's Guide* for information.
FFFF F110 0064	4	UI	Alarm 0: Is value a float? Yes = 1; no = 0. Yes is default.
FFFF F110 0068	18	–	Pad for alignment
FFFF F110 0080	4	B	Alarm 1: Deviation alarm: in alarm state? (Boolean)
FFFF F110 0084	4	B	Alarm 1: Enable deviation alarm (Boolean)
FFFF F110 0088	4	F	Alarm 1: Deviation alarm: previous deviation value (float)
FFFF F110 008C	4	F	Alarm 1: Deviation alarm, deviation amount (float)
FFFF F110 0090	8	M	Alarm 1: Deviation alarm reaction: set Scratch Pad bits on (mask)
FFFF F110 0098	8	M	Alarm 1: Deviation alarm reaction: set Scratch Pad bits off (mask)
FFFF F110 00A0	4	B	Alarm 1: High alarm: in alarm state? (Boolean)
FFFF F110 00A4	4	B	Alarm 1: Enable high alarm (Boolean)
FFFF F110 00A8	4	F	Alarm 1: High alarm setpoint
FFFF F110 00AC	4	F	Alarm 1: High alarm deadband
FFFF F110 00B0	8	M	Alarm 1: High alarm reaction: set Scratch Pad bits on (mask)
FFFF F110 00B8	8	M	Alarm 1: High alarm reaction: set Scratch Pad bits off (mask)
FFFF F110 00C0	4	B	Alarm 1: Low alarm: in alarm state? (Boolean)
FFFF F110 00C4	4	B	Alarm 1: Enable low alarm (Boolean)
FFFF F110 00C8	4	F	Alarm 1: Low alarm setpoint
FFFF F110 00CC	4	F	Alarm 1: Low alarm deadband
FFFF F110 00D0	8	M	Alarm 1: Low alarm reaction: set Scratch Pad bits on (mask)
FFFF F110 00D8	8	M	Alarm 1: Low alarm reaction: set Scratch Pad bits off (mask)
FFFF F110 00E0	4	UI	Alarm 1: Address of value to check. Use to set multiple alarms on one channel. See the *PAC Manager User's Guide* for information.
FFFF F110 00E4	4	UI	Alarm 1: Is value a float? Yes = 1; no = 0. Yes is default.
FFFF F110 00E8	18	–	Pad for alignment
Additional alarms follow in order on even 80 hex boundaries.			
FFFF F110 1F80	80	–	Alarm 63

Last valid address for this area: FFFF F110 1FFF

EVENT MESSAGE CONFIGURATION—READ/WRITE

PAC-R
PAC-S
EB
UIO
EIO
G4EB2

(Does not apply to *groov* I/O units or *groov* RIO modules.) See page 50 in this guide and the *PAC Manager User's Guide* for information on configuring messages as reactions to events or alarms. Only the first two messages are shown. Other messages follow the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F120 0000	4	UI	Message 0: Current message state. Messages become active when Scratch Pad conditions are met. To acknowledge receipt of an active message, write a 2 to this address. The message will not be sent again until the conditions are met again. 0 = Inactive, 1 = Active, 2 = Acknowledged

Starting Address	Length (hex)	Type	Description
FFFF F120 0004	8	M	Message 0: Scratch Pad bits on? (mask)
FFFF F120 000C	8	M	Message 0: Scratch Pad bits off? (mask)
FFFF F120 0014	4	B	Message 0: Enable streaming (Boolean). Be sure to fill in streaming configuration section. (See page 119.)
FFFF F120 0018	4	UI	Message 0: Stream period in seconds 0 = send once, 604800 = maximum
FFFF F120 001C	4	B	Message 0: Enable email (Boolean). Be sure to fill in email configuration section. (See page 143.)
FFFF F120 0020	4	UI	Message 0: Email period in seconds 0 = send once; 604800 = maximum
FFFF F120 0024	4	B	Message 0: Enable SNMP trap (Boolean). 0 = disable; non-0 = enable
FFFF F120 0028	4	UI	Message 0: SNMP trap period in seconds 0 = send once; 604800 = maximum
FFFF F120 002C	4	UI	Message 0: SNMP trap type
FFFF F120 0030	4	UI	Message 0: Priority. 0 = high; 1 = low. High is default. Applies only if you are using SNMP with a modem connection, and the I/O unit is dialing out.
FFFF F120 0034	4	–	Reserved
FFFF F120 0038	4	B	Message 0: Enable serial module message (Boolean). 0 = disable; non-0 = enable
FFFF F120 003C	4	M	Message 0: Serial ports to receive message (mask) Bits 0–31 correspond to ports 0–31.
FFFF F120 0040	80	S-ZT	Message 0: Message text. Limited to 127 characters. Used with email, serial, and (optional) SNMP messages. For memory map copying, source memory map address or data goes here. Plugins can be used in message text; see page 50 for information.
FFFF F120 00C0	4	UI	Message 1: Current message state 0 = Inactive, 1 = Active, 2 = Acknowledged
FFFF F120 00C4	8	M	Message 1: Scratch Pad bits on? (mask)
FFFF F120 00CC	8	M	Message 1: Scratch Pad bits off? (mask)
FFFF F120 00D4	4	B	Message 1: Enable streaming (Boolean). Be sure to fill in streaming configuration section. (See page 119.)
FFFF F120 00D8	4	UI	Message 1: Stream period in seconds 0 = send once, 604800 = maximum
FFFF F120 00DC	4	B	Message 1: Enable email (Boolean) Be sure to fill in email configuration section. (See page 143.)
FFFF F120 00E0	4	UI	Message 1: Email period in seconds 0 = send once; 604800 = maximum
FFFF F120 00E4	4	B	Message 1: Enable SNMP trap (Boolean). 0 = disable; non-0 = enable
FFFF F120 00E8	4	UI	Message 1: SNMP trap period in seconds 0 = send once; 604800 = maximum
FFFF F120 00EC	4	UI	Message 1: SNMP trap type
FFFF F120 00F0	4	UI	Message 1: Priority. 0 = high; 1 = low. High is default. Applies only if you are using SNMP with a modem connection, and the I/O unit is dialing out.
FFFF F120 00F4	4	–	Reserved

Starting Address	Length (hex)	Type	Description
FFFF F120 00F8	4	B	Message 1: Enable serial module message (Boolean). 0 = disable; non-0 = enable
FFFF F120 00FC	4	M	Message 1: Serial ports to receive message (mask) Bits 0–31 correspond to ports 0–31.
FFFF F120 0100	80	S-ZT	Message 1: Message text. Limited to 127 characters. Used with email, serial, and (optional) SNMP messages. For memory map copying, source memory map address or data goes here. Plugins can be used in message text; see page 50 for information.
Additional messages follow in order.			
FFFF F120 5F40	4	UI	Message 127: Current message state
FFFF F120 6000	1FFF	–	Reserved
FFFF F120 8000	4	UI	Message 0, memory map copying: Memory map address to copy data to (destination address), on the same or a different I/O unit.
FFFF F120 8004	4	IP	Message 0, memory map copying: IP address of destination I/O unit. Use 0.0.0.0 if copying to an address on the same I/O unit.
FFFF F120 8008	4	UI	Message 0, memory map copying: UDP port for destination I/O unit. (Ignored if same I/O unit.)
FFFF F120 800C	4	UI	Message 0, memory map copying: How often to copy data, in milliseconds. (0 = send once)
FFFF F120 8010	4	UI	Message 1, memory map copying: Memory map address to copy data to (destination address), on the same or a different I/O unit.
FFFF F120 8014	4	IP	Message 1, memory map copying: IP address of destination I/O unit. Use 0.0.0.0 if copying to an address on the same I/O unit.
FFFF F120 8018	4	UI	Message 1, memory map copying: UDP port for destination I/O unit. (Ignored if same I/O unit.)
FFFF F120 801C	4	UI	Message 1, memory map copying: How often to copy data, in milliseconds. (0 = send once)
Additional messages follow in order.			
FFFF F120 87F0	4	UI	Message 127, memory map copying: Memory map address to copy data to (destination address), on the same or a different I/O unit.
FFFF F120 9000	100	S-ZT	Message 0: Text of most recent message (read only)
FFFF F120 9100	4	UI	Message 0: Length of most recent message (read only)
FFFF F120 9104	100	S-ZT	Message 1: Text of most recent message (read only)
FFFF F120 9204	4	UI	Message 1: Length of most recent message (read only)
Additional messages follow in order.			

Last valid address for this area: FFFF F121 11FF

EMAIL CONFIGURATION—READ/WRITE

PAC-R
PAC-S
EB
UIO
EIO
G4EB2

Use this section to set up email addresses to which the I/O unit will send event messages or logged data. (Does not apply to *groov* I/O units or *groov* RIO modules.) Also use "Event Message Configuration—Read/Write" on page 141 to set up the messages or "Data Logging Configuration—Read/Write" on page 154

to set up data logging. See Chapter 2: Overview of Programming for more information on configuring events and messages and logging data.

Starting Address	Length (hex)	Type	Description
FFFF F130 0000	4		IP address of the SMTP mail server the I/O unit will use to send email.
FFFF F130 0004	4	UI	SMTP port number for sending messages (usually 25).
FFFF F130 0008	32	S-ZT	TO: Email address of the person to receive the message.
FFFF F130 003A	32	S-ZT	FROM: Email address of the I/O unit. Use an address that will identify the I/O unit to the recipient of the message.
FFFF F130 006C	32	S-ZT	RE: Subject of the email. Plugins are allowed. See page 50 for more information.
FFFF F130 00A0	4	UI	Timeout: the length of time in milliseconds the I/O unit should wait for a response from the email server. Default is 30,000. On PAC-R and EB, if no connection is made, the device stores up to 129 messages. When communication is restored, all stored messages are sent.

SERIAL EVENT CONFIGURATION—READ/WRITE

PAC-R
EB
UIO
EIO

(Does not apply to *groov* I/O units, *groov* RIO modules, SB brains, or SNAP Simple I/O) Use this section to set up events for serial communication modules attached to the SNAP Ethernet-based I/O unit. For more information on serial communication modules, see the *SNAP Serial Communication Module User's Guide* (form 1191). For more information on serial events and reactions, see page 49.

Before you configure serial events, configure the serial modules. (See page 107.) In the following table, only the first two events are shown. Other events follow the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F154 0000	4	M	Serial Event 0: Serial port mask. Bits 0-31 correspond to ports 0-31. On bits represent serial ports to monitor for the event string. Event occurs if *any* of the ports receives the event string. NOTE: A null entry here disables this entry and any higher numbered entries.
FFFF F154 0004	4	–	Reserved
FFFF F154 0008	4	UI	Serial Event 0: SNMP trap type (if sending an SNMP trap as a reaction to the serial event)
FFFF F154 000C	4	UI	Serial Event 0: SNMP trap period—how often, in seconds, to send the trap as a reaction to the serial event
FFFF F154 0010	28	S-ZT	Serial Event 0: Pattern string for the event. Wildcards (* and ?) are allowed.
FFFF F154 0038	28	S-ZT	Serial Event 0: Reaction string to be sent with the SNMP trap. Plug-ins allowed ($!_str_ or $!_port_ and others). See page 50 for more information.
FFFF F154 0060	8	M	Serial Event 0: Scratch Pad bits to turn on
FFFF F154 0068	8	M	Serial Event 0: Scratch Pad bits to turn off
FFFF F154 0070	4	UI	Serial Event 0: Enable email message (0 = Disable, 1 = Enable)
FFFF F154 0074	4	M	Serial Event 1: Serial port mask. Bits 0-31 correspond to ports 0-31. On bits represent serial ports to monitor for the event string. Event occurs if *any* of the ports receives the event string. NOTE: A null entry here disables this entry and any higher numbered entries.
FFFF F154 0074	4	–	Reserved

Starting Address	Length (hex)	Type	Description
FFFF F154 007C	4	UI	Serial Event 1: SNMP trap type (if sending an SNMP trap as a reaction to the serial event)
FFFF F154 0080	4	UI	Serial Event 1: SNMP trap period—how often, in seconds, to send the trap as a reaction to the serial event
FFFF F154 0084	28	S-ZT	Serial Event 1: Pattern string for the event. Wildcards (* and ?) are allowed.
FFFF F154 00AC	28	S-ZT	Serial Event 1: Reaction string to be sent with the SNMP trap. Plug-ins allowed ($!_str_ or $!_port_ and others). See page 50 for more information.
FFFF F154 00D4	8	M	Serial Event 1: Scratch Pad bits to turn on
FFFF F154 00DC	8	M	Serial Event 1: Scratch Pad bits to turn off
FFFF F154 00E4	4	UI	Serial Event 1: Enable email message (0 = Disable, 1 = Enable)
Additional events follow in order.			
FFFF F154 0E80	4	UI	Serial Event 0: SNMP trap priority. High = 0; low = 1. High is default. Applies only if you are using SNMP with a modem connection, and the I/O unit is dialing out.
FFFF F154 0E84	4	UI	Serial Event 1: SNMP trap priority (0 = High, 1 = Low)
FFFF F154 0E88	4	UI	Serial Event 2: SNMP trap priority (0 = High, 1 = Low)
Trap priority addresses for additional events follow in order.			
FFFF F154 0F00	4	UI	Serial Event 0: Disable SNMP trap (0 = No, 1 = Yes)
FFFF F154 0F04	4	UI	Serial Event 1: Disable SNMP trap (0 = No, 1 = Yes)
FFFF F154 0F08	4	UI	Serial Event 2: Disable SNMP trap (0 = No, 1 = Yes)
Disable trap addresses for additional events follow in order.			
Last valid address for this area: FFFF F154 0EFC			

WIEGAND SERIAL EVENT CONFIGURATION—READ/WRITE

PAC-REB UIO EIO

Use this section to set up events for Wiegand serial communication modules attached to the SNAP Ethernet-based I/O unit. (Does not apply to *groov* I/O units or *groov* RIO modules.) For more information on Wiegand modules, see the *SNAP Serial Communication Module User's Guide* (form 1191). For more information on serial events and reactions, see page 49.

Before you configure Wiegand serial events, configure the Wiegand modules. (See page 108.) In the following table, only the first two events are shown. Other events follow the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F156 0000	4	M	Wiegand Event 0: Wiegand port mask. Bits 0-31 correspond to ports 0-31. On bits represent serial ports to monitor for the event string. Event occurs if *any* of the ports receives the event string. NOTE: A null entry here disables this entry and any higher numbered entries.
FFFF F156 0004	4	–	Reserved
FFFF F156 0008	4	UI	Wiegand Event 0: SNMP trap type (if sending an SNMP trap as a reaction to the serial event)
FFFF F156 000C	4	UI	Wiegand Event 0: SNMP trap period—how often, in seconds, to send the trap as a reaction to the serial event

Starting Address	Length (hex)	Type	Description
FFFF F156 0010	28	S-ZT	Wiegand Event 0: Pattern string for the event. Wildcards (* and ?) are allowed.
FFFF F156 0038	28	S-ZT	Wiegand Event 0: Reaction string to be sent with the SNMP trap. Plug-ins allowed ($!_str_ or $!_port_ and others). See page 50 for more information.
FFFF F156 0060	8	M	Wiegand Event 0: Scratch Pad bits to turn on
FFFF F156 0068	8	M	Wiegand Event 0: Scratch Pad bits to turn off
FFFF F156 0070	4	UI	Wiegand Event 0: Enable email message (0 = Disable, 1 = Enable)
FFFF F156 0074	4	M	Wiegand Event 1: Wiegand port mask. Bits 0–31 correspond to ports 0–31. On bits represent ports to monitor for the event string. Event occurs if *any* of the ports receives the event string. NOTE: A null entry here disables this entry and any higher numbered entries.
FFFF F156 0078	4	–	Reserved
FFFF F156 007C	4	UI	Wiegand Event 1: SNMP trap period—how often, in seconds, to send the trap as a reaction to the event
FFFF F156 0080	4	UI	Wiegand Event 1: SNMP trap type (if sending an SNMP trap as a reaction to the event)
FFFF F156 0084	28	S-ZT	Wiegand Event 1: Pattern string for the event. Wildcards (* and ?) are allowed.
FFFF F156 00AC	28	S-ZT	Wiegand Event 1: Reaction string to be sent with the SNMP trap. Plug-ins allowed ($!_str_ or $!_port_ and others). See page 50 for more information.
FFFF F156 00D4	8	M	Wiegand Event 1: Scratch Pad bits to turn on
FFFF F156 00DC	8	M	Wiegand Event 1: Scratch Pad bits to turn off
FFFF F156 00E4	4	UI	Wiegand Event 1: Enable email message (0 = Disable, 1 = Enable)
Additional events follow in order.			
FFFF F156 0E80	4	UI	Wiegand Event 0: SNMP trap priority. High = 0; low = 1. High is default. Applies only if you are using SNMP with a modem connection, and the I/O unit is dialing out. See the device's user guide for details.
FFFF F156 0E84	4	UI	Wiegand Event 1: SNMP trap priority (0 = High, 1 = Low)
FFFF F156 0E88	4	UI	Wiegand Event 2: SNMP trap priority (0 = High, 1 = Low)
Trap priority addresses for additional events follow in order.			
FFFF F156 0F00	4	UI	Wiegand Event 0: Disable SNMP trap (0 = No, 1 = Yes)
FFFF F156 0F04	4	UI	Wiegand Event 1: Disable SNMP trap (0 = No, 1 = Yes)
FFFF F156 0F08	4	UI	Wiegand Event 2: Disable SNMP trap (0 = No, 1 = Yes)
Disable SNMP traps for additional events follow in order.			
Last valid address for this area: FFFF F156 0F7F			

HIGH-DENSITY DIGITAL—READ ONLY

PR1
RIO
PAC-R
EB
SB
UIO
EIO
SIO

Use this section to read the state of channels on *groov* I/O, *groov* RIO, and SNAP high-density digital input and output modules on the I/O unit; also use it to read latches and counters for high-density input channels.

IMPORTANT: *For state and latches, data is shown in 64-bit masks. The lower 32 bits correspond to the 32 channels on the module, with bit 0 representing channel 0. The upper 32 bits are not currently used. For example, for Module 0 channel state, addresses F1808000 through F1808003 will be zero-filled; address F1808004 will contain data for channels 31 through 24, and so on.*

Starting Address	Length (hex)	Type	Description
FFFF F180 8000	8	M	Module 0: Channel state. 0 = Off; 1 = On
FFFF F180 8008	8	M	Module 0: On-latch state. 0 = Off; 1 = On
FFFF F180 8010	8	M	Module 0: Off-latch state. 0 = Off; 1 = On
FFFF F180 8018	28	–	Module 0: Reserved
FFFF F180 8040	8	M	Module 1: Channel state. 0 = Off; 1 = On
FFFF F180 8048	8	M	Module 1: On-latch state. 0 = Off; 1 = On
FFFF F180 8050	8	M	Module 1: Off-latch state. 0 = Off; 1 = On
FFFF F180 8058	28	–	Module 1: Reserved
Additional modules follow in order on even 40 hex boundaries.			
FFFF F180 83C0	8	M	Module 15: Channel state. 0 = Off; 1 = On
FFFF F180 83C8	8	M	Module 15: On-latch state. 0 = Off; 1 = On
FFFF F180 83D0	8	M	Module 15: Off-latch state. 0 = Off; 1 = On
FFFF F180 83D8	28	–	Module 15: Reserved
FFFF F180 9000	4	UI	Module 0, Channel 0 (0,0): Counter value
FFFF F180 9004	4	UI	0,1: Counter value
FFFF F180 9008	4	UI	0,2: Counter value
Additional channels follow in order on even 4 hex boundaries.			
FFFF F180 9100	4	UI	1,0: Counter value
FFFF F180 9104	4	UI	1,1: Counter value
FFFF F180 9108	4	UI	1,2; Counter value
Additional channels and modules follow in order.			
FFFF F180 9F00	4	UI	15,0: Counter value
Last valid address for this area: FFFF F180 9FFE			

HIGH-DENSITY DIGITAL READ AND CLEAR—READ/WRITE

PR1
RIO
PAC-R
EB
SB
UIO
EIO
SIO

Reading: When you read data from this area, the data for all *groov* I/O, *groov* RIO, and SNAP high-density digital channels is returned as a mask, with a 1 in every position where the latch is set. Then all latches are cleared.

Writing: To clear individual latches using this area, read the latches first if needed (see "High-Density Digital—Read Only" on page 147). Then write a mask to this area with a 1 in each position you want to clear. (0 is ignored.)

IMPORTANT: *Latch data is shown in 64-bit masks. The lower 32 bits correspond to the 32 channels on the module, with bit 0 representing channel 0. The upper 32 bits are not currently used. For example, for Module 0 on-latch state,*

addresses F180A000 through F180A003 will be zero-filled; address F180A004 will contain data for channels 31 through 24, and so on.

Starting Address	Length (hex)	Type	Description
FFFF F180 A000	8	M	Module 0: On-latch state. Reading: 0 = Off; 1 = On Writing: 0 = Ignore, 1 = Clear
FFFF F180 A008	8	M	Module 0: Off-latch state. 0 = Off; 1 = On Writing: 0 = Ignore, 1 = Clear
FFFF F180 A010	10	–	Module 0: Reserved
FFFF F180 A020	8	M	Module 1: On-latch state. 0 = Off; 1 = On Writing: 0 = Ignore, 1 = Clear
FFFF F180 A028	8	M	Module 1: Off-latch state. 0 = Off; 1 = On Writing: 0 = Ignore, 1 = Clear
FFFF F180 A030	10	–	Module 1: Reserved
Additional modules follow in order on even 20 hex boundaries.			
FFFF F180 A1E0	8	M	Module 15: On-latch state. 0 = Off; 1 = On Writing: 0 = Ignore, 1 = Clear
FFFF F180 A1E8	8	M	Module 15: Off-latch state. 0 = Off; 1 = On Writing: 0 = Ignore, 1 = Clear
FFFF F180 A1F0	10	–	Module 15: Reserved
FFFF F180 B000	4	UI	Module 0, Channel 0 (0,0): Returns counter value and sets counter to zero.
FFFF F180 B004	4	UI	0,1: Returns counter value and sets counter to zero.
FFFF F180 B008	4	UI	0,2: Returns counter value and sets counter to zero.
Additional channels follow in order on even 4 hex boundaries.			
FFFF F180 B100	4	UI	1,0: Returns counter value and sets counter to zero.
FFFF F180 B104	4	UI	1,1: Returns counter value and sets counter to zero.
FFFF F180 B108	4	UI	1,2: Returns counter value and sets counter to zero.
Additional channels and modules follow in order.			
FFFF F180 BF00	4	UI	15,0: Returns counter value and sets counter to zero.
Last valid address for this area: FFFF F180 BFFE			

HIGH-DENSITY DIGITAL WRITE—READ/WRITE

PR1
RIO
PAC-R
EB
SB
UIO
EIO
SIO

Use this section to write to *groov* I/O, *groov* RIO, and SNAP high-density digital output modules. Data is sent in 64-bit masks. The lower 32 bits correspond to the 32 channels on the module, with bit 0 representing channel 0. The upper 32 bits are not currently used. For example, the On mask for Module 0 would appear as shown in the following table:

This address	Contains this data
F180C000	Zero-filled (not currently used)
F180C001	
F180C002	
F180C003	

F180C004	Channels 31–24
F180C005	Channels 23–16
F180C006	Channels 15–8
F180C007	Channels 7–0

NOTE: If the same bit is set in both the On mask and the Off mask, the channel will be turned off.

Starting Address	Length (hex)	Type	Description
FFFF F180 C000	8	M	Module 0: On mask (bitmask representing channels to turn on.) 1 = Turn on; 0 = Ignore
FFFF F180 C008	8	M	Module 0: Off mask (bitmask representing channels to turn off.) 1 = Turn off; 0 = Ignore
FFFF F180 C010	30	–	Module 0: Reserved
FFFF F180 C040	8	M	Module 1: On mask (bitmask representing channels to turn on.) 1 = Turn on; 0 = Ignore
FFFF F180 C048	8	M	Module 1: Off mask (bitmask representing channels to turn off.) 1 = Turn off; 0 = Ignore
FFFF F180 C050	30	–	Module 1: Reserved
Additional modules follow in order on even 40 hex boundaries.			
FFFF F180 C3C0	8	M	Module 15: On mask (bitmask representing channels to turn on.) 1 = Turn on; 0 = Ignore
FFFF F180 C3C8	8	M	Module 15: Off mask (bitmask representing channels to turn off.) 1 = Turn off; 0 = Ignore
FFFF F180 C3D0	30	–	Module 15: Reserved
Last valid address for this area: FFFF F180 C3FE			

PID CONFIGURATION AND STATUS—READ/WRITE

PR1
RIO
PAC-R
EB
SB
UIO
EIO

Use this section to configure proportional/integral/ derivative (PID) loops to run on the I/O unit and to check PID status. (For configuring PID *modules*, see page 156.) For additional information on using PID loops, see page 55. Number of PID loops available depends on the I/O unit: there are 4 on *groov* RIO, 16 on SNAP Ethernet, 32 on SNAP Ultimate, and 96 on *groov* I/O, SNAP PAC R-series, and SNAP PAC EB I/O units.

The first table shows addresses for current algorithm values and status flags. The second table includes scanned values and configuration addresses. In both tables, only the first two PIDs are shown. Others follow the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F200 0000	4	F	PID 0: Current value for Error (Input – Setpoint)
FFFF F200 0004	4	F	PID 0: Current value for P (gain) contribution
FFFF F200 0008	4	F	PID 0: Current value for I (integral) contribution
FFFF F200 000C	4	F	PID 0: Current value for D (derivative) contribution
FFFF F200 0010	4	F	PID 0: Current value for Integral
FFFF F200 0014	14	–	Reserved for internal use
FFFF F200 0028	4	UI	PID 0: Scan counter
FFFF F200 002C	4	UI	PID 0: Status flags: 1 = Input is below Input low scale; 2 = Input is above Input high scale; 4 = Output has been forced to a predetermined level because input is out of range.
FFFF F200 0030	4	UI	PID 0: Status bits ON. Used to control individual Status flag bits. Write a 1 to turn the bit on.
FFFF F200 0034	4	UI	PID 0: Status bits OFF. Used to control individual Status flag bits. Write a 1 to clear the bit.

Starting Address	Length (hex)	Type	Description
FFFF F200 0038	4	F	PID 0: Current input value when input is provided by a host (application or supervisory system). When F210 0044 is set to zero, meaning that the input value is coming from a host, the host writes the Input value here. Applies only to Velocity C algorithm and SNAP firmware R8.5e or higher.
FFFF F200 003C	14	–	Reserved
FFFF F200 0050	4	F	PID 1: Current value for Error (Input – Setpoint)
FFFF F200 0054	4	F	PID 1: Current value for P (gain) contribution
FFFF F200 0058	4	F	PID 1: Current value for I (integral) contribution
FFFF F200 005C	4	F	PID 1: Current value for D (derivative) contribution
FFFF F200 0060	4	F	PID 1: Current value for Integral
FFFF F200 0064	14	–	Reserved for internal use
FFFF F200 0078	4	UI	PID 1: Scan counter
FFFF F200 007C	4	UI	PID 1: Status flags: 1 = PV low; 2 = PV high; 4 = output forced
FFFF F200 0080	4	UI	PID 1: Status bits ON. Used to control individual Status flag bits. Write a 1 to turn the bit on.
FFFF F200 0084	4	UI	PID 1: Status bits OFF. Used to control individual Status flag bits. Write a 1 to clear the bit.
FFFF F200 0088	4	F	PID 1: Current input value when input is provided by a host (application or supervisory system). When F210 0044 is set to zero, meaning that the input value is coming from a host, the host writes the Input value here. Applies only to Velocity C algorithm and SNAP firmware R8.5e or higher.
FFFF F200 008C	14	–	Reserved

Additional PIDs follow in order on even 50 hex boundaries.
See additional PID addresses in the table below.)

Last valid address for this area: FFFF F200 2EDF

This second table shows scanned values and configuration addresses. Only the first two PIDs are shown. Others follow the same pattern.

This area is stored to flash.

Starting Address	Length (hex)	Type	Description
FFFF F210 0000	4	F	PID 0: Input or process variable (PV) value. If the value at memory map address F2100044 is not zero, the value at that address is copied into this location prior to each PID calculation.
FFFF F210 0004	4	F	PID 0: Setpoint value. If the value at memory map address F2100048 is not zero, the value at that address is copied into this location prior to each PID calculation.
FFFF F210 0008	4	F	PID 0: Current value of feed forward
FFFF F210 000C	4	F	PID 0: Current value of Output
FFFF F210 0010	4	F	PID 0: Tuning: P (Gain) value. Should be positive for cooling, negative for heating.
FFFF F210 0014	4	F	PID 0: Tuning: I (Integral) value, in units of one per second. Increase value to increase contribution.

Starting Address	Length (hex)	Type	Description
FFFF F210 0018	4	F	PID 0: Tuning: D (Derivative) value, in seconds. Increase value to increase contribution.
FFFF F210 001C	4	F	PID 0: Tuning: Feed forward gain
FFFF F210 0020	4	F	PID 0: Configuration: Maximum output change allowed. Zero disables this feature.
FFFF F210 0024	4	F	PID 0: Configuration: Minimum output change allowed. Zero disables this feature.
FFFF F210 0028	4	F	PID 0: Scaling: Input low range
FFFF F210 002C	4	F	PID 0: Scaling: Input high range
FFFF F210 0030	4	F	PID 0: Scaling: Output lower clamp
FFFF F210 0034	4	F	PID 0: Scaling: Output upper clamp
FFFF F210 0038	4	F	PID 0: Configuration: PID scan time in seconds. Minimum value is 0.001 (1 millisecond).
FFFF F210 003C	4	F	PID 0: Configuration: If Input (PV) is below low range, output is set to this value.
FFFF F210 0040	4	F	PID 0: Configuration: If Input (PV) is above high range, output is set to this value.
FFFF F210 0044	4	UI	PID 0: Input memory map address for PID input or cascading PIDs. Specifies the memory map address from which the input value is copied to F2100000 prior to each PID calculation. If this address is 0, no input value is copied, and the input value must be written directly to F2100038 by an application. Use 0 when supervisory system supplies or processes this value.
FFFF F210 0048	4	UI	PID 0: For cascading PIDs. Specifies the memory map address from which the setpoint value is copied to F2100004 prior to each PID calculation. If this address is 0, no setpoint value is copied, and the setpoint value must be written directly to F2100004 by an application. Use 0 when supervisory system supplies or processes this value.
FFFF F210 004C	4	UI	PID 0: For cascading PIDs. Specifies the memory map address to which the output value is written after each PID calculation. If this address is 0, the output value is not written. Use 0 when supervisory system supplies or processes this value.
FFFF F210 0050	4	UI	PID 0: Configuration: Algorithm choice. 0 = PID disabled 1 = Velocity algorithm (Type B; deprecated) 2 = ISA algorithm (Obsolete) 3 = Parallel algorithm (Obsolete) 4 = Interacting algorithm (Obsolete) 5 = Velocity algorithm (Type C; SNAP firmware R8.5e and higher) 6 = ISA algorithm (SNAP firmware R9.4c or higher) 7 = Parallel algorithm (SNAP firmware R9.4c or higher) 8 = Interaction algorithm (SNAP firmware R9.4c or higher)
FFFF F210 0054	4	UI	PID 0: Configuration: Manual mode. 1 = Yes; 0 = No
FFFF F210 0058	4	UI	PID 0: Configuration flags: 1 = Enable square root of Input. 2 = Force output when Input is out of range. Set range in addresses F210 0028 and F210 002C. 4 = Switch to manual mode when input goes out of range.
FFFF F210 005C	4	UI	PID 0: Configuration bits ON. Used to control individual Configuration flag bits. Write a 1 to turn the bit on.
FFFF F210 0060	4	UI	PID 0: Configuration bits OFF. Used to control individual Configuration flag bits. Write a 1 to clear the bit.

Starting Address	Length (hex)	Type	Description
FFFF F210 0064	4	F	PID 0: Current value at the memory map address from which the input value is copied.
FFFF F210 0068	4	F	PID 0: Current value at the memory map address from which the set-point value is copied.
FFFF F210 006C	14	–	Reserved
FFFF F210 0080	4	F	PID 1: Input or process variable (PV) value. If the value at memory map address F21000C4 is not zero, the value at that address is copied into this location prior to each PID calculation.
FFFF F210 0084	4	F	PID 1: Setpoint value. If the value at memory map address F21000C8 is not zero, the value at that address is copied into this location prior to each PID calculation.
FFFF F210 0088	4	F	PID 1: Current value of feed forward
FFFF F210 008C	4	F	PID 1: Current value of Output
FFFF F210 0090	4	F	PID 1: Tuning: P (Gain) value. Should be positive for cooling, negative for heating.
FFFF F210 0094	4	F	PID 1: Tuning: I (Integral) value, in units of one per second. Increase value to increase contribution.
FFFF F210 0098	4	F	PID 1: Tuning: D (Derivative) value, in seconds. Increase value to increase contribution.
FFFF F210 009C	4	F	PID 1: Tuning: Feed forward gain
FFFF F210 00A0	4	F	PID 1: Configuration: Maximum output change allowed. Zero disables this feature.
FFFF F210 00A4	4	F	PID 1: Configuration: Minimum output change allowed. Zero disables this feature.
FFFF F210 00A8	4	F	PID 1: Scaling: Input low range
FFFF F210 00AC	4	F	PID 1: Scaling: Input high range
FFFF F210 00B0	4	F	PID 1: Scaling: Output lower clamp
FFFF F210 00B4	4	F	PID 1: Scaling: Output upper clamp
FFFF F210 00B8	4	F	PID 1: Configuration: PID scan time in seconds. Minimum value is 0.001 (1 millisecond).
FFFF F210 00BC	4	F	PID 1: Configuration: If Input (PV) is below low range, output is set to this value.
FFFF F210 00C0	4	F	PID 1: Configuration: If Input (PV) is above high range, output is set to this value.
FFFF F210 00C4	4	UI	PID 1: Input memory map address for PID input or cascading PIDs. Specifies the memory map address from which the input value is copied to F2100000 prior to each PID calculation. If this address is 0, no input value is copied, and the input value must be written directly to F2100038 by an application. Use 0 when supervisory system supplies or processes this value.
FFFF F210 00C8	4	UI	PID 1: For cascading PIDs. Specifies the memory map address from which the setpoint value is copied to F2100084 prior to each PID calculation. If this address is 0, no setpoint value is copied, and the setpoint value must be written directly to F2100084 by an application. Use 0 when supervisory system supplies or processes this value.
FFFF F210 00CC	4	UI	PID 1: For cascading PIDs. Specifies the memory map address to which the output value is written after each PID calculation. If this address is 0, the output value is not written. Use 0 when supervisory system supplies or processes this value.

Starting Address	Length (hex)	Type	Description
FFFF F210 00D0	4	UI	PID 1: Configuration: Algorithm choice. 0 = PID disabled 1 = Velocity algorithm (Type B; deprecated) 2 = ISA algorithm (Obsolete) 3 = Parallel algorithm (Obsolete) 4 = Interacting algorithm (Obsolete) 5 = Velocity algorithm (Type C; SNAP firmware R8.5e and higher) 6 = ISA algorithm (SNAP firmware R9.4c or higher) 7 = Parallel algorithm (SNAP firmware R9.4c or higher) 8 = Interaction algorithm (SNAP firmware R9.4c or higher)
FFFF F210 00D4	4	UI	PID 1: Configuration: Manual mode. 1 = Yes; 0 = No
FFFF F210 00D8	4	UI	PID 1: Configuration flags: 1 = Enable square root of Input. 2 = Force output when Input is out of range. Set range at addresses F210 00A8 and F210 00AC. 4 = Switch to manual mode when input goes out of range.
FFFF F210 00DC	4	UI	PID 1: Configuration bits ON. Used to control individual Configuration flag bits. Write a 1 to turn the bit on.
FFFF F210 00E0	4	UI	PID 1: Configuration bits OFF. Used to control individual Configuration flag bits. Write a 1 to clear the bit.
FFFF F210 00E4	4	F	PID 1: Current value at the memory map address from which the input value is copied.
FFFF F210 00E8	4	F	PID 1: Current value at the memory map address from which the set-point value is copied.
FFFF F210 00EC	14	–	Reserved

Additional PIDs follow in order on even 80 hex boundaries.

Last valid address for this area: FFFF F210 47FF

PUBLIC TAG CONFIGURATION—READ/WRITE

PR1
RIO

Use this section to configure which I/O channels are published as tags (public tags) that can be used by the MQTT Service in *groov* Manage. Bits in the mask allow a channel and some of its features to be published.

If an I/O channel is public, it is always readable. Channels marked writeable in the bitmask can have all features written to (for example, a discrete input can be marked writeable so that its on and off latches can be cleared).

Discrete bitmask attributes are as follows:

Bit Index	Discrete values	Description
0	State (Read)	For a tag to be public, this value must be 1. All values are readable.
1	Writeable	When this bit is set, all values are writeable.
2	On-Latch	When writeable, a write clears the on-latch.
3	Off-Latch	When writeable, a write clears the off-latch.
4	Counter	When writeable, a write clears the counter.
5–31	reserved	

Analog bitmask attributes are:

Bit Index	Analog values	Description
0	State (Read)	For a tag to be public, this value must be 1. All values are readable.
1	Writeable	When this bit is set, all values are writeable.
2	Maximum	When writeable, a write clears the analog maximum value.
3	Minimum	When writeable, a write clears the analog minimum value.
4	Analog Quality	
5–31	reserved	

Only the first two channels on module 0 are shown below. Other modules and channels follow the same pattern, to a total of 16 modules, each with 32 channels.

Starting Address	Length (hex)	Type	Description
FFFF F228 0000	4	UI	Module 0, Channel 0; Bitmask I/O attributes. Area is stored to Flash.
FFFF F228 0004	4	F	Module 0, Channel 0; Analog value deadband. The amount of change before an update is published.
FFFF F228 0008	78	--	Module 0, Channel 0; Reserved (120 bytes)
FFFF F228 0080	4	UI	Module 0, Channel 1; Bitmask I/O attributes
FFFF F228 0084	4	F	Module 0, Channel 1; Analog value deadband. The amount of change before an update is published
FFFF F228 0088	78	--	Module 0, Channel 1; Reserved (120 bytes)
Additional modules and channels follow in order on even 80 hex boundaries.			
Last valid address for this area: FFFF F228 FFFF			

Starting Address	Length (hex)	Type	Description
FFFF F2290000	4	UI	Public tag version number. Automatically incremented by the OptoMMP command processor each time any area of 0xF2280000 changes, or if the channel's name or units changes. Value is not persistent; it resets when the I/O unit restarts.

DATA LOGGING CONFIGURATION—READ/WRITE

PAC-R
EB
SB
UIO
EIO
G4EB2

(Does not apply to *groov* I/O units or *groov* RIO modules.) Use this section to configure up to 64 memory map addresses you wish to log data from (log points). The values from all log points go into the same data log file, which you can access using the data log section of the memory map (page 155). Data from this composite file can be emailed; to do so, also use page 143 to set up email. See page 54 for more information on data logging.

Only the first three log points are shown. Other log points follow the same pattern.

Starting Address	Length (hex)	Type	Description
FFFF F300 0000	8	M	Log Point 0: Scratch Pad bits on? (mask)
FFFF F300 0008	8	M	Log Point 0: Scratch Pad bits off? (mask)
FFFF F300 0010	4	UI	Log Point 0: Memory map address to log data from
FFFF F300 0014	4	UI	Log Point 0: Data format of value to be logged

Starting Address	Length (hex)	Type	Description
FFFF F300 0018	4	UI	Log Point 0: How often to log the value, in milliseconds (If you change this interval, you must save to flash and restart the I/O unit.)
FFFF F300 001C	8	M	Log Point 1: Scratch Pad bits on? (mask)
FFFF F300 0024	8	M	Log Point 1: Scratch Pad bits off? (mask)
FFFF F300 002C	4	UI	Log Point 1: Memory map address to log data from
FFFF F300 0030	4	UI	Log Point 1: Data format of value to be logged
FFFF F300 0034	4	UI	Log Point 1: How often to log the value, in milliseconds (If you change this interval, you must save to flash and restart the I/O unit.)
FFFF F300 0038	8	M	Log Point 2: Scratch Pad bits on? (mask)
FFFF F300 0040	8	M	Log Point 2: Scratch Pad bits off? (mask)
FFFF F300 0048	4	UI	Log Point 2: Memory map address to log data from
FFFF F300 004C	4	UI	Log Point 2: Data format of value to be logged
FFFF F300 0050	4	UI	Log Point 2: How often to log the value, in milliseconds (If you change this interval, you must save to flash and restart the I/O unit.)
Additional log points follow in order.			
FFFF F300 0700	4	B	Enable email for sending data log file. Applies to ALL log points. Also configure email (page 143).
FFFF F300 0704	4	UI	Number of data log entries in each email message. Applies to ALL log points.

Last valid address for this area: FFFF F300 0707

DATA LOG—READ/WRITE

PAC-REB SB **UIO** EIO G4EB2

(Does not apply to *groov* I/O units, *groov* RIO modules, or SNAP Simple I/O) Use this section to access data logged from memory map addresses set up in "Data Logging Configuration—Read/Write" on page 154. The data from all addresses goes into one data log file. The data log is a circular buffer; it holds 300 samples of 14 bytes (hex) per entry, and the newest data item replaces the oldest one. See "Logging Data" on page 54 for more information on data logging, and see page 55 for how to interpret information from these data log addresses.

Although this area is read/write, you would normally read it only. You could write to it to clear it, however.

Starting Address	Length (hex)	Type	Description
FFFF F302 0000	14	*	First entry in the data log
FFFF F302 0014	14	*	Second entry in the data log
Additional entries follow in order.			
FFFF F302 175C	14	*	Last entry in the data log

Last valid address in this area: FFFF F302 176F

* Binary data. See page 55.

PID MODULE CONFIGURATION—READ/WRITE

PAC-RUIO EIO

(Does not apply to *groov* I/O units or *groov* RIO modules.) Use this area to configure PID modules on the rack. (**NOTE:** PID modules are at their end of life and are *not recommended* for new development. Instead, use PID loops that run on the I/O unit. To configure PID loops, see page 149.)

The table shows addresses for a PID module in rack position zero. Modules in other positions on the rack follow the same pattern and start on even 100 hex boundaries.

CAUTION: *Values for many of these memory map addresses require you to calculate them in advance. Some values are read-only and cannot be changed. For explanations and important information on using these addresses, see the* SNAP PID Module User's Guide *(form 1263).*

Starting Address	Length (hex)	Type	Description
FFFF F400 0000	4	I	PID module in position 0 on the rack: Control word
FFFF F400 0004	4	I	Position 0: State of status flags (read only)
FFFF F400 0008	4	I	Position 0: Scantime base (scantime resolution)
FFFF F400 000C	4	I	Position 0: Scantime multiplier
FFFF F400 0010	4	I	Position 0: TPO period multiplier
FFFF F400 0014	4	I	Position 0: Output
FFFF F400 0018	4	I	Position 0: Tune PID: proportional (gain)
FFFF F400 001C	4	I	Position 0: Tune PID: integral ratio
FFFF F400 0020	4	I	Position 0: Tune PID: derivative ratio
FFFF F400 0024	4	I	Position 0: Setpoint
FFFF F400 0028	4	I	Position 0: Process variable
FFFF F400 002C	4	I	Position 0: Filter exponential
FFFF F400 0030	4	I	Position 0: Setpoint low limit
FFFF F400 0034	4	I	Position 0: Setpoint high limit
FFFF F400 0038	4	I	Position 0: Process low limit
FFFF F400 003C	4	I	Position 0: Process high limit
FFFF F400 0040	4	I	Position 0: Output low limit
FFFF F400 0044	4	I	Position 0: Output high limit
FFFF F400 0048	4	I	Position 0: Output slew rate
FFFF F400 004C	4	I	Position 0: Output limit deadband
FFFF F400 0050	4	I	Position 0: Current PID (read only)
FFFF F400 0054	4	I	Position 0: Last PID (read only)
FFFF F400 0058	4	I	Position 0: Oldest PID (read only)
FFFF F400 005C	4	I	Position 0: Current PID error (read only)
FFFF F400 0060	4	I	Position 0: Last PID error (read only)
FFFF F400 0064	4	I	Position 0: Output change (read only)
FFFF F400 0068	4	I	Position 0: Output value (read only)
FFFF F400 006C	4	I	Position 0: Scantime countdown (read only)
FFFF F400 0100	4	I	PID module in position 1 on the rack: Control word
Additional modules follow in order on even 100 hex boundaries.			
FFFF F400 0F00	4	I	PID module in position 15 on the rack: Control word

Last valid address for this area: FFFF F400 0F6F

CONTROL ENGINE—READ/WRITE

PAC-R PAC-S

Use this section to view and change features in R-series and S-series PACs only. For more information on these features, see the the *PAC Control User's Guide* (form 1700).

Starting Address	Length (hex)	Type	Description
FFFF F408 0000	4	UI	Control engine operation. 0 = control engine disabled; 1 = control engine enabled. On a PAC R controller, disabling the control engine means all processor resources are available for use by the brain.
FFFF F408 0004	4	UI	Control engine feature. 0 = No feature; 1 = background downloading; 2 = secure strategy downloads; 3 = redundant controller (Do not set the redundant controller feature here; use the PAC Redundancy Manager software in PAC Project Professional 9.0 or newer to set it.)

Last valid address in this area: FFFF F408 0007

SERIAL BRAIN COMMUNICATION—READ/WRITE

SB

Use this section with SNAP PAC SB brains. only

Starting Address	Length (hex)	Type	Description
FFFF F700 2000	4	UI	Turnaround time delay, port 0. Number of ms the brain should wait before sending the response back to the host.
FFFF F700 2100	4	B	Communications debug flag. 1 = communication error blink codes are enabled; 0 = communication error blink codes are disabled. These blink codes help in troubleshooting. Do not leave them enabled for normal operation, as they slow down processing speed. See the brain user's guide for more information.

Last valid address in this area: FFFF F700 2103

MICROSD CARD—READ/WRITE

PAC-R PAC-S

Use this section with microSD cards in R-series and S-series PACs only. Also see address F030 0230 in the "Status Area Read—Read Only" section (page 92). See the PAC's user guide for additional information on using microSD cards.

Starting Address	Length (hex)	Type	Description
FFFF F700 2200	4	B	Enable/disable use of microSD card to update firmware and strategies. Non-zero = enabled; 0 = disabled. Default is enabled. Requires SNAP firmware R8.4a or newer.
FFFF F700 2204	4	UI	Number of bytes free on the microSD card (capacity <= 2GB). Requires SNAP firmware R8.5a or newer.
FFFF F700 2208	8	UI	Number of bytes free on the microSDHC card (capacity > 2GB and <= 32GB). Requires SNAP firmware R9.6a or newer.

Last valid address in this area: FFFF F700 220F

WLAN STATUS—READ ONLY

PAC-R
PAC-S
EB

Wired+Wireless SNAP PAC models only.

Use this section to read status information for SNAP PAC controllers and brains communicating over a wireless LAN. Also see "WLAN Enable—Read/Write" on page 160 and "WLAN Configuration—Read/Write" on page 159.

Starting Address	Length (hex)	Type	Description
FFFF F700 3000	2	–	Pad for alignment
FFFF F700 3002	6	UI	MAC address for WLAN interface
FFFF F700 3008	4	UI	WLAN state: 0 = disconnected, 1 = inactive, 2 = scanning, 3 = associating, 4 = associated, 5 = WPA 4-way handshake, 6 = WPA group handshake, 7 = completed
FFFF F700 300C	2	–	Pad for alignment
FFFF F700 300E	6	UI	ID for current BSS (basic service set), if WLAN state = completed
FFFF F700 3014	20	S-ZT	SSID (service set identifier) of current BSS, if WLAN state = completed
FFFF F700 3034	4	UI	Channel frequency (MHz)
FFFF F700 3038	4	UI	Rate at which data is received (kbps)
FFFF F700 303C	4	UI	Rate at which data is transmitted (kbps)
FFFF F700 3040	4	UI	Signal to noise ratio (dB)
FFFF F700 3044	4	I	Signal level (dBm)
FFFF F700 3048	4	I	Noise level (dBm)
FFFF F700 304C	4	UI	Number of missed beacon frames
FFFF F700 3050	4	UI	Number of connection events
FFFF F700 3054	4	UI	Number of disconnection events
FFFF F700 3058	4	UI	Number of low signal strength events
FFFF F700 305C	4	UI	Total packets received
FFFF F700 3060	4	UI	Total packets transmitted
FFFF F700 3064	4	UI	Total bytes received
FFFF F700 3068	4	UI	Total bytes transmitted
FFFF F700 306c	4	UI	Bad packets received
FFFF F700 3070	4	UI	Packet transmit problems
FFFF F700 3074	4	UI	Incoming packets dropped due to resource constraints
FFFF F700 3078	4	UI	Outgoing packets dropped due to resource constraints
FFFF F700 307c	4	UI	Received packets that were too long or too short
FFFF F700 3080	4	UI	Received packets with wrong network ID/SSID
FFFF F700 3084	4	UI	Unable to code/decode (WEP)
FFFF F700 3088	4	UI	Can't perform MAC reassembly
FFFF F700 308C	4	UI	Maximum MAC retries reached

Last valid address in this area: FFFF F700 308F

WLAN CONFIGURATION—READ/WRITE

PAC-R
PAC-S
EB

Wired+Wireless SNAP PAC models only. Use this section to configure wireless LAN communication parameters. You must store to flash memory and cycle power after any configuration change. For security reasons, some addresses in this section are write only; if you try to read them, 0xFF is returned.

NOTE: As with all Ethernet devices, only one default gateway is in use at a time. This default gateway is always the gateway configured for the highest priority active interface (active means it has a link and is capable of communication). Default gateways are prioritized from highest to lowest priority through the following interfaces:

1. *PPP*
2. *Ethernet 0*
3. *Ethernet 1*
4. *WLAN*

Also see "WLAN Enable—Read/Write" on page 160 and "WLAN Status—Read Only" on page 158.

Starting Address	Length (hex)	Type	Description
FFFF F700 4000	4	UI	Enable/disable wireless network configuration. 0=disabled, 1=enabled. Default is disabled; must be enabled for the WLAN to work. In addition, address F800 0000 must also be enabled to use the wireless network.
FFFF F700 4004	4	IP	IP address for the wireless interface
FFFF F700 4008	4	IP	Subnet mask for the wireless interface
FFFF F700 400C	4	IP	Default Gateway IP address for the wireless interface
FFFF F700 4010	4	IP	Secondary Gateway IP address for the wireless interface
FFFF F700 4014	4	IP	Primary DNS Server IP address for the wireless interface
FFFF F700 4018	4	IP	Secondary DNS Server IP address for the wireless interface
FFFF F700 401C	24	S-ZT	Service Set Identifier (SSID, or network name). Use a literal string enclosed in double quotes, max. 32 ASCII characters inside the quotes. Or use an ASCII hex string (each ASCII character represented by two hex digits) with no quotes. Examples: Literal string in double quotes: "Hello" Equivalent ASCII hex string, no quotes: 48656C6C6F NULL=Any SSID.
FFFF F700 4040	4	–	Reserved
FFFF F700 4044	4	UI	IEEE 802.11 operation mode: 0=Infrastructure mode, 1=Ad-hoc (IBSS) mode.
FFFF F700 4048	4	UI	Security protocol: 1=WPA/TKIP encryption 2=WPA2/CCMP encryption
FFFF F700 404C	4	UI	Authenticated key management protocol: 2=WPA-PSK 4=Plain text (unencrypted) or static WEP 16=Ad-hoc TKIP/CCMP encryption
FFFF F700 4050	4	UI	IEEE 802.11 authentication algorithm: 1=Open System Authentication, required by WPA/WPA2 2=Shared Key Authentication (less secure, WEP only)
FFFF F700 4054	4	UI	Unicast cipher for WPA: 1=Group keys (ad-hoc), 2=64-bit WEP key, 4=128-bit WEP key, 8=TKIP encryption, 16=AES encryption
FFFF F700 4058	4	UI	Broadcast/multicast cipher for WPA: 1=Group keys (ad-hoc), 2=64-bit WEP key, 4=128-bit WEP key, 8=TKIP encryption, 16=AES encryption

Starting Address	Length (hex)	Type	Description
FFFF F700 405C	44	S-ZT	WPA 256-bit pre-shared key: Use 64 hex digits (32 bytes, no quotes; may represent an ASCII string or binary data). Or use ASCII passphrase (8 to 63 characters within double quotes). Set to 0xFF if unused.
FFFF F700 40A0	24	S-ZT	(Write only) Static WEP key0: Use 10 hex or 26 hex digits (5 or 13 bytes, no quotes). Or use ASCII passphrase (5 or 13 characters within double quotes).
FFFF F700 40C4	24	S-ZT	(Write only) Static WEP key1: Use 10 hex or 26 hex digits (5 or 13 bytes, no quotes). Or use ASCII passphrase (5 or 13 characters within double quotes).
FFFF F700 40E8	24	S-ZT	(Write only) Static WEP key2: Use 10 hex or 26 hex digits (5 or 13 bytes, no quotes). Or use ASCII passphrase (5 or 13 characters within double quotes).
FFFF F700 410C	24	S-ZT	(Write only) Static WEP key3: Use 10 hex or 26 hex digits (5 or 13 bytes, no quotes). Or use ASCII passphrase (5 or 13 characters within double quotes).
FFFF F700 4130	4	UI	Default WEP key: 0=WEP key0, 1=WEP key1, 2=WEP key2, 3=WEP key3.
FFFF F700 4134	4	UI	Channel for ad-hoc mode. Example: 2412 = 802.11b/g channel 1. See list of channels.
FFFF F700 413C	2C4	–	Pad for alignment

Addresses F7004400 through F700553B are reserved.

Last valid address in this area: FFFF F700 553B

WLAN ENABLE—READ/WRITE

PAC-R
PAC-S
EB

Wired+Wireless SNAP PAC models only.

Use this section to enable wireless LAN communications. Also see "WLAN Configuration—Read/Write" on page 159 and "WLAN Status—Read Only" on page 158.

Starting Address	Length (hex)	Type	Description
FFFF F800 0000	4	B	Wireless LAN communication. 0=Disable, 1=Enable. Default is disabled.
FFFF F800 0004	4	UI	WLAN logging to /sdcard0/ath0.log (requires microSD card). 0=Disabled; 1=Log errors and warnings; 2=Log debug information
FFFF F800 0008	4	UI	Inactivity timeout for received Ethernet packets on WLAN interface (in seconds). 0=disabled. Provides recovery for an invalid association. If this timer expires, unit will disassociate, re-scan, and associate.

Last valid address in this area: FFFF F800 000B

IP SETTINGS—READ/WRITE

PAC-R
PAC-S
EB
G4EB2

(Does not apply to *groov* I/O units or *groov* RIO modules.) If you are not using PAC Manager to change IP addressing for the Ethernet network interface(s) on the device, you can use this area of the memory map to do so. **All changes made in this area require two steps** (PAC Manager does these steps automatically):

1. Send the new address (8 bytes consisting of the address [4 bytes] plus the 1s complement of it [4 bytes]). *All 8 bytes must be sent in one transaction.* The 1s complement is required to avoid accidental changes.
2. Send a reset hardware command (see Status Area Write address F0380000, operation code 0x00000005) to cycle power and make the changes take effect.

Starting Address	Length (hex)	Type	Description
FFFF FFFF F008	8	IP	IP address for interface 0 (primary IP address).
FFFF FFFF F010	8	IP	Subnet mask for interface 0
FFFF FFFF F018	8	IP	Primary default gateway address for interface 0
FFFF FFFF F020	8	IP	Primary DNS server address for interface 0
FFFF FFFF F028	40	–	Reserved
FFFF FFFF F050	8	IP	Secondary IP address (PAC-S & PAC-R only)
FFFF FFFF F058	8	IP	Secondary IP subnet mask (PAC-S & PAC-R only)
FFFF FFFF F060	8	IP	(Read only) Secondary MAC address (PAC-S & PAC-R only)
FFFF FFFF F068	8	IP	Secondary IP default gateway address (PAC-S & PAC-R only)
FFFF FFFF F070	8	IP	Secondary IP DNS server address (PAC-S & PAC-R only)

Last valid address in this area: FFFF FFFF F077

B: Rack and Module Compatibility

The following table shows rack and module compatibility for Opto 22 memory-mapped I/O processors, on-the-rack controllers, brains, and brain boards.

Product Family	Part Number	Chassis/ Mounting rack	Modules per mounting rack	Module family	Maximum modules allowed per I/O unit (largest chassis/rack)
***groov* EPIC processors**	GRV-EPIC-PR1	GRV-EPIC-CHS4 GRV-EPIC-CHS8 GRV-EPIC-CHS16	4, 8 or 16	*groov* I/O	Up to 16 analog, digital, and serial *groov* I/O modules[1]
***groov* RIO modules**	GRV-R7-MM1001-10	n/a	1	*groov* RIO	1
SNAP PAC R-series on-the-rack controllers	SNAP-PAC-R1 SNAP-PAC-R1-FM SNAP-PAC-R1-W	SNAP-PAC-RCK4[2] SNAP-PAC-RCK4-FM SNAP-PAC-RCK8 SNAP-PAC-RCK8-FM SNAP-PAC-RCK12 SNAP-PAC-RCK12-FM SNAP-PAC-RCK16 SNAP-PAC-RCK16-FM	4, 8, 12, or 16	SNAP I/O	16 4-channel digital 16 analog 8 serial 16 high-density digital
	SNAP-PAC-R2 SNAP-PAC-R2-FM SNAP-PAC-R2-W				16 4-channel digital[3] 16 analog 8 serial 16 high-density digital
	SNAP-PAC-R1-B	SNAP-B racks	4, 8, 12, or 16	SNAP I/O	8 4-ch digital (first 8 slots) 16 analog 8 serial 16 high-density digital
SNAP PAC EB brains	SNAP-PAC-EB1 SNAP-PAC-EB1-FM SNAP-PAC-EB1-W	SNAP-PAC-RCK4[2] SNAP-PAC-RCK4-FM SNAP-PAC-RCK8 SNAP-PAC-RCK8-FM SNAP-PAC-RCK12 SNAP-PAC-RCK12-FM SNAP-PAC-RCK16 SNAP-PAC-RCK16-FM	4, 8, 12, or 16	SNAP I/O	16 4-channel digital 16 analog 8 serial 16 high-density digital
	SNAP-PAC-EB2 SNAP-PAC-EB2-FM SNAP-PAC-EB2-W				16 4-channel digital[3] 16 analog 8 serial 16 high-density digital
SNAP PAC SB brains	SNAP-PAC-SB1 SNAP-PAC-SB1-FM	SNAP-PAC-RCK4[2] SNAP-PAC-RCK4-FM SNAP-PAC-RCK8 SNAP-PAC-RCK8-FM SNAP-PAC-RCK12 SNAP-PAC-RCK12-FM SNAP-PAC-RCK16 SNAP-PAC-RCK16-FM	4, 8, 12, or 16	SNAP I/O	16 4-channel digital 16 analog 16 high-density digital
	SNAP-PAC-SB2				16 4-channel digital[3] 16 analog 16 high-density digital

Product Family	Part Number	Chassis/ Mounting rack	Modules per mounting rack	Module family	Maximum modules allowed per I/O unit (largest chassis/rack)
SNAP Simple I/O	SNAP-ENET-S64	SNAP-M16[2] SNAP-M32 SNAP-M48 SNAP-M64	4, 8, 12, or 16	SNAP I/O	16 4-channel digital[3] 16 analog 8 serial 16 high-density digital
SNAP Ethernet I/O	SNAP-B3000-ENET SNAP-ENET-RTC	SNAP-B racks	4, 8, 12, or 16	SNAP I/O	8 4-ch digital (first 8 slots) 16 analog 8 serial 16 high-density digital
	SNAP-ENET-D64	SNAP-D64RS	16	SNAP I/O	16 4-channel digital[3]
SNAP Ultimate I/O	SNAP-UP1-ADS	SNAP-B racks	4, 8, 12, or 16	SNAP I/O	8 4-ch digital (first 8 slots) 16 analog 8 serial 16 high-density digital
	SNAP-UP1-M64	SNAP-M16[2] SNAP-M32 SNAP-M48 SNAP-M64	4, 8, 12, or 16	SNAP I/O	16 4-channel digital[3] 16 analog 8 serial 16 high-density digital
	SNAP-UP1-D64	SNAP-D64RS	16	SNAP I/O	16 4-channel digital[3]
E1 Brain Board	E1	Digital G4PB series[4] Digital PB series[4] for G1 or Quad Pak	G4:16 G1:16 Quad Pak: 4	G4 G1 Quad Pak	G4: 16 digital G1: 16 digital Quad Pak: 4
E2 Brain Board	E2	Analog PB series	G1:16	G1	G1: 16 analog
G4EB2 brains	G4EB2	G4PB32H PB32HQ	G4: 32 Quad Pak: 4	G4 Quad Pak	G4: 32 digital Quad Pak: 4
	G4D32EB2	(Included)	32	G4	32 digital
	G4D32EB2-UPG	G4D32RS digital brick	32	G4	32 digital

[1] No more than four *groov* serial modules per chassis. Analog, digital, and serial *groov* I/O modules can be combined on the same *groov* EPIC chassis. Serial modules are supported only in the first four slots in the chassis. Maximum number of modules may be fewer when GRV-OVMALC-8 modules are configured for current loops. For information about power consumption by module, see the groov *EPIC Power Supplies, Converters, and Adapters* data sheet (form 2246).
[2] SNAP PAC racks and M-series racks can be used interchangeably.
[3] Digital channel features are simplified.
[4] E1 brain boards also work with PB and G4PB integral racks.

For additional compatibility information about SNAP PAC devices (such as the specific modules supported by each device), see the *Legacy and Current Product Comparison and Compatibility Charts* (form 1693).

C: SNAP Features Comparison Chart

SNAP PAC PROCESSORS AND FEATURES

Some of the features mentioned in this guide apply to some models and not others. See data sheets for details.

E1 and E2 brain boards have additional features if they are used with the Optomux protocol. For details, see the *E1 and E2 User's Guide* (form 1563).
A few features listed in this table are not available through the OptoMMP memory map; they require PAC Control commands.

Key

[0] E1 brain up to 400 Hz. High-density digital modules up to 50 Hz. Four channel SNAP modules vary; check specifications.
[1] Four-channel SNAP digital modules only; speed depends on module specifications. Not available on high-density digital modules.
[2] Requires a SNAP quadrature input module (SNAP-IDC5Q).
[3] Requires PAC Control commands (PAC Control Pro 8.2 or higher or PAC Control Basic 9.0 or higher) and a SNAP PAC controller.
[4] Requires a SNAP analog TPO module (SNAP-AOD-29).
[5] Compatible with PAC Control using firmware 7.1 or higher; however, several 8.x features are not available.
[6] Converts OptoControl strategies to PAC Control, when used with PAC Control Professional.
[7] FTP client provided by PAC Control strategy.
[8] Applies to SNAP-ENET-RTC, not to SNAP-B3000-ENET.
[9] Available when used with OptoOPCServer, PAC Control, and a SNAP PAC controller.
[10] As provided by the Microsoft Windows computer the software runs on.

Feature		SoftPAC Software -based PAC	Current Hardware															Legacy Hardware								
			SNAP PAC Controller								SNAP PAC Brain								E1 Brain Board	E2 Brain Board	SNAP Simple	SNAP Ethernet		SNAP Ultimate		
			SNAP-PAC-S1 SNAP-PAC-S1-FM	SNAP-PAC-S1-W	SNAP-PAC-S2	SNAP-PAC-S2-W	SNAP-PAC-R1 SNAP-PAC-R1-B SNAP-PAC-R1-FM	SNAP-PAC-R1-W	SNAP-PAC-R2 SNAP-PAC-R2-FM	SNAP-PAC-R2-W	SNAP-PAC-EB1 SNAP-PAC-EB1-FM	SNAP-PAC-EB1-W	SNAP-PAC-EB2 SNAP-PAC-EB2-FM	SNAP-PAC-EB2-W	SNAP-PAC-SB1	SNAP-PAC-SB2	G4EB2			SNAP-ENET-S64	SNAP-B3000-ENET SNAP-ENET-RTC	SNAP-ENET-D64	SNAP-UP1-ADS	SNAP-UP1-D64	SNAP-UP1-M64
Digital I/O Channels	Input latching	n/a	n/a				●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	●
	Watchdog timer						●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	●
	On/off status						●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	●
	Low-speed counting[0]						●	●			●	●			●			●			●		●		
	High-speed counting (up to 20 kHz)[1]						●	●			●	●			●						●		●		
	Quadrature counting[2]						●	●			●	●			●						●		●		
	On-pulse and off-pulse measurement[1]						●	●			●	●			●						●		●		
	Frequency and period measurement						●	●			●	●			●										
	TPO (time-proportional output)						●	●	●	●	●	●	●	●	●	●	●				●		●		
	Pulse generation (N pulses, continuous square wave, on-pulse, off-pulse)						●	●	●	●	●	●	●	●	●	●	●				●		●		
	Digital totalizing						●	●	●	●	●	●	●	●	●	●	●								
Analog I/O channels	Thermocouple linearization (32-bit floating point for linearized values)	n/a	n/a				●	●	●	●	●	●	●	●	●	●				●	●	●		●	●
	Minimum/maximum values						●	●	●	●	●	●	●	●	●	●				●	●	●		●	●
	Offset and gain						●	●	●	●	●	●	●	●	●	●				●	●	●		●	●
	Scaling						●	●	●	●	●	●	●	●	●	●				●	●	●		●	●
	TPO (Time-proportional output)[4]						●	●	●	●	●	●	●	●	●	●					●	●		●	●
	Output clamping						●	●	●	●	●	●	●	●	●	●				●	●	●		●	●
	Filter weight						●	●	●	●	●	●	●	●	●	●					●	●		●	●
	Watchdog timer						●	●	●	●	●	●	●	●	●	●					●	●		●	●
	Ramping[3]						●	●	●	●	●	●	●	●	●	●				●		●		●	
	Analog totalizing[3]						●	●	●	●	●	●	●	●	●	●									
SNAP high-density digital modules		n/a	n/a				●	●	●	●	●	●	●	●	●	●					●	●		●	●
SNAP analog modules with more than 4 channels							●	●	●	●	●	●	●	●	●	●					●			●	●
Serial communication modules							●	●	●	●	●	●	●	●							●	●		●	●

Feature	SoftPAC Software -based PAC	Current Hardware															Legacy Hardware								
		SNAP PAC Controller									SNAP PAC Brain							E1 Brain Board	E2 Brain Board	SNAP Simple	SNAP Ethernet		SNAP Ultimate		
		SNAP-PAC-S1 SNAP-PAC-S1-FM	SNAP-PAC-S1-W	SNAP-PAC-S2	SNAP-PAC-S2-W	SNAP-PAC-R1 SNAP-PAC-R1-B SNAP-PAC-R1-FM	SNAP-PAC-R1-W	SNAP-PAC-R2 SNAP-PAC-R2-FM	SNAP-PAC-R2-W	SNAP-PAC-EB1 SNAP-PAC-EB1-FM	SNAP-PAC-EB1-W	SNAP-PAC-EB2 SNAP-PAC-EB2-FM	SNAP-PAC-EB2-W	SNAP-PAC-SB1	SNAP-PAC-SB2	G4EB2			SNAP-ENET-S64	SNAP-B3000-ENET SNAP-ENET-RTC	SNAP-ENET-D64	SNAP-UP1-ADS	SNAP-UP1-D64	SNAP-UP1-M64
Ethernet network	●	●	●	●	●	●	●	●	●	●	●	●	●			●	●	●	●	●	●	●	●	●	●
Two independent Ethernet interfaces (two IP addresses)	10	●	●	●	●	●	●	●	●																
Two switched Ethernet interfaces (one IP address)										●	●	●	●			●									
One wireless LAN interface (separate IP address)			●		●		●		●		●		●												
Serial network (RS-485/422)		●	●	●	●									●	●		●	●							
Serial ports (RS-232) for PPP or serial devices		●	●	●	●	●	●	●	●														●	●	●
OptoMMP protocol	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Optomux protocol (over Ethernet or serial)																	●	●							
Modbus/TCP		●	●	●	●	●	●	●	●	●	●	●	●			●	●	●	●	●	●	●	●	●	●
EtherNet/IP (Allen-Bradley® Logix PLCs)		●	●	●	●	●	●	●	●	●	●	●	●			●									
RESTful API		●	●	●	●	●	●	●	●																
HTTP/HTTPS		●	●	●	●	●	●	●	●																
UDP Streaming		●	●	●	●	●	●	●	●	●	●	●	●			●			●	●	●	●	●	●	●
SNMP (network management)		●	●	●	●	●	●	●	●	●	●	●	●			●				●	●	●	●	●	●
PPP (dial-up modems)		●	●	●	●	●	●	●	●											●	●	●	●	●	●
FTP server		●	●	●	●	●	●	●	●	●	●	●	●			●						●	●	●	●
FTP client[7]	●					●	●	●	●													●	●	●	●
Email (SMTP client)	●					●	●	●	●	●	●	●	●			●				●	●	●	●	●	●
OPC driver	●					●	●	●	●	●	●	●	●	●[9]	●[9]	●	●	●	●	●	●	●	●	●	●
Security for wireless network (WPA2-AES, WPA-TKIP, WEP)	10		●		●		●		●		●		●												
Security for wired Ethernet network (IP filtering, port access)	10	●	●	●	●	●	●	●	●	●	●	●	●			●	●	●	●	●	●	●	●	●	●
Runs PAC Control strategies	●	●	●	●	●	●	●	●	●													●[5]	●[5]	●[5]	

Feature		SoftPAC Software -based PAC	Current Hardware															Legacy Hardware								
			SNAP PAC Controller								SNAP PAC Brain															
			SNAP-PAC-S1 SNAP-PAC-S1-FM	SNAP-PAC-S1-W	SNAP-PAC-S2	SNAP-PAC-S2-W	SNAP-PAC-R1 SNAP-PAC-R1-B SNAP-PAC-R1-FM	SNAP-PAC-R1-W	SNAP-PAC-R2 SNAP-PAC-R2-FM	SNAP-PAC-R2-W	SNAP-PAC-EB1 SNAP-PAC-EB1-FM	SNAP-PAC-EB1-W	SNAP-PAC-EB2 SNAP-PAC-EB2-FM	SNAP-PAC-EB2-W	SNAP-PAC-SB1	SNAP-PAC-SB2	G4EB2	E1 Brain Board	E2 Brain Board	SNAP Simple SNAP-ENET-S64	SNAP Ethernet SNAP-B3000-ENET SNAP-ENET-RTC	SNAP Ethernet SNAP-ENET-D64	SNAP Ultimate SNAP-UP1-ADS	SNAP Ultimate SNAP-UP1-D64	SNAP Ultimate SNAP-UP1-M64
Compatible with PAC Control (using SNAP PAC controller)		●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Legacy software support	Runs ioControl strategies	●	●	●	●	●	●	●	●	●														●	●	●
	Compatible with ioControl (through SNAP PAC, SNAP-LCE, or SNAP Ultimate controller running ioControl)	●	●	●	●	●	●	●	●	●								●	●	●	●	●	●	●	●	●
	Compatible with OptoControl (through Opto 22 controller with Ethernet card)		6	6	6	6	6	6	6	6										●	●	●				
PID logic on the brain							●	●	●	●	●	●	●	●	●	●					●		●		●	●
Number of PIDs available							96	96	96	96	96	96	96	96	96	96					16		32		32
Digital events		n/a	n/a				●	●	●	●	●	●	●	●	●	●	●				●[1]	●[1]	●[1]	●[1]	●[1]
Alarm events							●	●	●	●	●	●	●	●	●	●					●		●		●
Serial events							●	●	●	●	●	●	●	●							●		●		●
Event messages							●	●	●	●	●	●	●	●			●				●	●	●	●	●
Data logging in the brain		n/a	n/a				●	●	●	●	●	●	●	●			●				●		●		●
I/O channel data mirroring							●	●	●	●	●	●	●	●			●				●		●		●
Memory map data copying							●	●	●	●	●	●	●	●			●				●		●		●
Scratch Pad area (peer-to-peer communication) Bits Floats Strings Integers (32 bit) Integers (64 bit)		● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●	● ● ● ● ●				●		● ● ● ● ●	● ● ● ● ●	● ● ● ● ●
Realtime clock (RTC)		10	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●				●[8]		●	●	●

D: *groov* EPIC and *groov* RIO Features and Comparison Charts

In this appendix:

groov RIO FEATURES

The following table lists channels on the GRV-R7-MM1001-10 and the features they offer. To configure channel features, see page 31. Note that some signal types are available only on specific channels, as listed in the "Channels" row.

IMPORTANT: Thermocouple inputs and discrete sinking outputs cannot be mixed on channels 0–3.

GRV-R7-MM1001-10	Signal Type						
	DI: • Discrete DC • Switch Input, Powered	**DI:** • Discrete DC • Switch Input, Powered	**DO:** • DC Sinking	**DO (Mech. Relay):** • Form C	**AI:** • Voltage • ICTD	**AI:** • Current • Thermocouple • Millivolt	**AO:** • Voltage • Current
Channels	**0-1**	**2-7**	**0-7**	**8-9**	**0-7**	**0-3**	**4-7**
Features							
On/off State	x	x	x	x			
On/off Latching	x						
Counting	x						
On/off Totalization	x						
Frequency Measurement	x						
Period Measurement	x						
Pulse Measurement	x						
Quadrature							
Scaling					x	x	x
Offset and Gain					x	x	
Minimum/Maximum Values					x	x	
Average Filter Weight					x	x	
Simple Moving Average							
Analog Totalizing					x	x	

GRV-R7-MM1001-10	Signal Type						
	DI: • Discrete DC • Switch Input, Powered	**DI:** • Discrete DC • Switch Input, Powered	**DO:** • DC Sinking	**DO (Mech. Relay):** • Form C	**AI:** • Voltage • ICTD	**AI:** • Current • Thermocouple • Millivolt	**AO:** • Voltage • Current
Channels	**0-1**	**2-7**	**0-7**	**8-9**	**0-7**	**0-3**	**4-7**
Output Pulsing / TPO			x				
Ramping							x
Clamping							x
Watchdog Timeout Value			x	x			x
Problem Indication					x	x	x

groov EPIC SYSTEM FEATURES

The following table lists *groov* I/O modules and the features they offer. To configure channel features, see "Configuring Channel Features" on page 31.

Features		On/off state	On/off latching	Frequency measurement	Period measurement	Pulse measurement	Counting / Quadrature Counting	Output pulsing	On/off totalization	Channel-to-channel isolation	Analog totalizing	Watchdog timer	Scaling	Minimum/maximum values	Offset and gain	Average filter weight	Quality Indicator (see next page)	Clamping
Discrete input																		
GRV-IAC-24	AC input, 24 channels, 85–140 VAC	●	●	●	●	●	●		●									
GRV-IACDCTTL-24	AC/DC input, 24 channels, 2–16 V AC/DC	●	●	●	●	●	●		●									
GRV-IACDCTTLS-24	AC/DC input, 24 channels, 2–16 V AC/DC, on/off state only	●																
GRV-IACHV-24	AC input, 24 channels, 120–280 VAC	●	●	●	●	●	●		●									
GRV-IACHVS-24	AC input, 24 channels, 120–280 VAC, on/off state only	●																
GRV-IACI-12	AC input, 12 channels, 85–140 VAC	●	●	●	●	●	●		●	●								
GRV-IACIHV-12	AC input, 12 channels, 120–280 VAC	●	●	●	●	●	●		●	●								
GRV-IACIHVS-12	AC input, 12 channels, 120–280 VAC, on/off state only	●								●								
GRV-IACIS-12	AC input, 12 channels, 85–140 VAC, on/off state only	●								●								
GRV-IACS-24	AC input, 24 channels, 85–140 VAC, on/off state only	●																
GRV-IDC-24	DC input, 24 channels, 15–30 V	●	●	●	●	●	●		●									

Features		On/off state	On/off latching	Frequency measurement	Period measurement	Pulse measurement	Counting / Quadrature Counting	Output pulsing	On/off totalization	Channel-to-channel isolation	Analog totalizing	Watchdog timer	Scaling	Minimum/maximum values	Offset and gain	Average filter weight	Quality Indicator (see next page)	Clamping
GRV-IDCI-12	DC input, 12 channels, 10–30 V	●	●	●	●	●	●		●	●								
GRV-IDCIS-12	DC input, 12 channels, 10–30 V, on/off status only	●								●								
GRV-IDCS-24	DC input, 24 channels, 15–30 V, on/off status only	●																
Analog input																		
GRV-IMA-24	Analog current input, 24 channels, configurable ranges										●			●	●	●	●	
GRV-ITMI-8	Analog input, 8 channel, thermocouple or mV									●	●			●	●	●	●	
GRV-IV-24	Analog voltage input, 24 channels, 7 configurable ranges										●			●	●	●	●	
Discrete output																		
GRV-OAC-12	AC discrete output, 12 channels, 12–250 VAC	●						●	●			●					●	
GRV-OACI-12	AC discrete output, 12 channels, 12–250 VAC	●						●	●	●		●					●	
GRV-OACIS-12	AC discrete output, 12 channels, 12–250 VAC, on/off only	●								●		●						
GRV-OACS-12	AC discrete output, 12 channels, 12–250 VAC, on/off only	●										●						
GRV-ODCI-12	DC discrete output, 12 channels, 5–60 VDC	●						●	●	●		●						
GRV-ODCIS-12	DC discrete output, 12 channels, 5–60 VDC, on/off only	●								●		●						
GRV-ODCSRC-24	DC discrete output, 24 channels, 5–60 VDC, sourcing	●										●						
GRV-OMRIS-8	AC/DC discrete output, 8 channels, mechanical relay, 5 A	●										●						
Analog output																		
GRV-OVMALC-8	Analog output, 8 ch., voltage or current, chassis-powered loop											●					●	●

QUALITY INDICATORS

groov I/O modules and *groov* RIO channels that report quality continuously poll for current data values and identify deviations between reported and expected values. For example, when a channel on a GRV-IV-24 reports a value greater than 10% above range, the module sets a quality indicator code 15 (Input is more than

10% above the maximum range) on the channel. When the issue is resolved, the quality indicator code returns to 0 (zero).

The following is a list of valid quality indicator codes and their definitions.

0 = Data quality is good. No exception conditions occurred.

9 = Digital output is on, but current is not flowing. May indicate an open circuit or blown fuse in field equipment.

15 = Analog input is above 110% of channel's range. Applicable to unipolar (zero and positive values only) and bipolar (can include negative and positive values) signal ranges.

16 = Analog input is below -110% of channel's range. Applicable to unipolar (zero and positive values only) and bipolar (can include negative and positive values) signal ranges.

18 = Analog output fault.

- When configured for voltage, indicates the load resistance is too low (that is, the load is drawing too much current to maintain the voltage).
- When configured for current, indicates very high resistance or possible open current loop.

21 = Analog output is at the positive range limit. Applicable only when the value written exceeds the maximum limit. Indicates the module has clamped the output to the limit. Can be caused by a configuration or logic error; for example, the strategy sent a value to the channel that is above the channel's maximum range.

22 = Analog output is at the minus range limit. Applicable only when the value written exceeds the minimum limit. Indicates the module has clamped the output to the limit. Can be caused by a configuration or logic error; for example, the strategy sent a value to the channel that is below the channel's minimum range.

30 = Node not found.

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